

Mockingbird-N/V/L 14/15_CML & Hellcat14/15_CML UMA Schematic

2019/12/09
REV : SC



DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

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<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

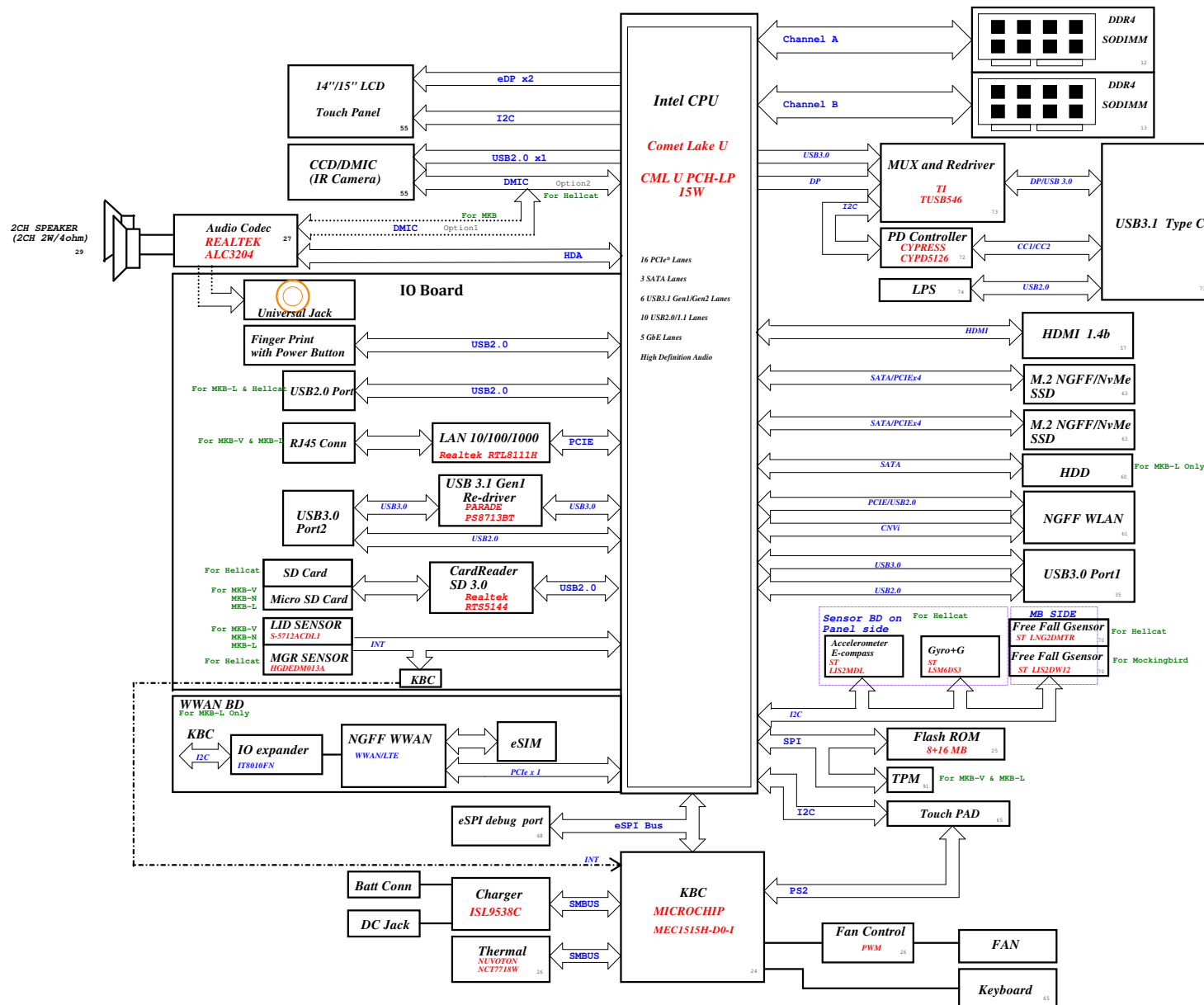
Mockingbird_CML

Rev
SC

Date: Monday, December 09, 2019

Sheet 1 of 105

Mockingbird N/V/L/HellCat CML Block Diagram

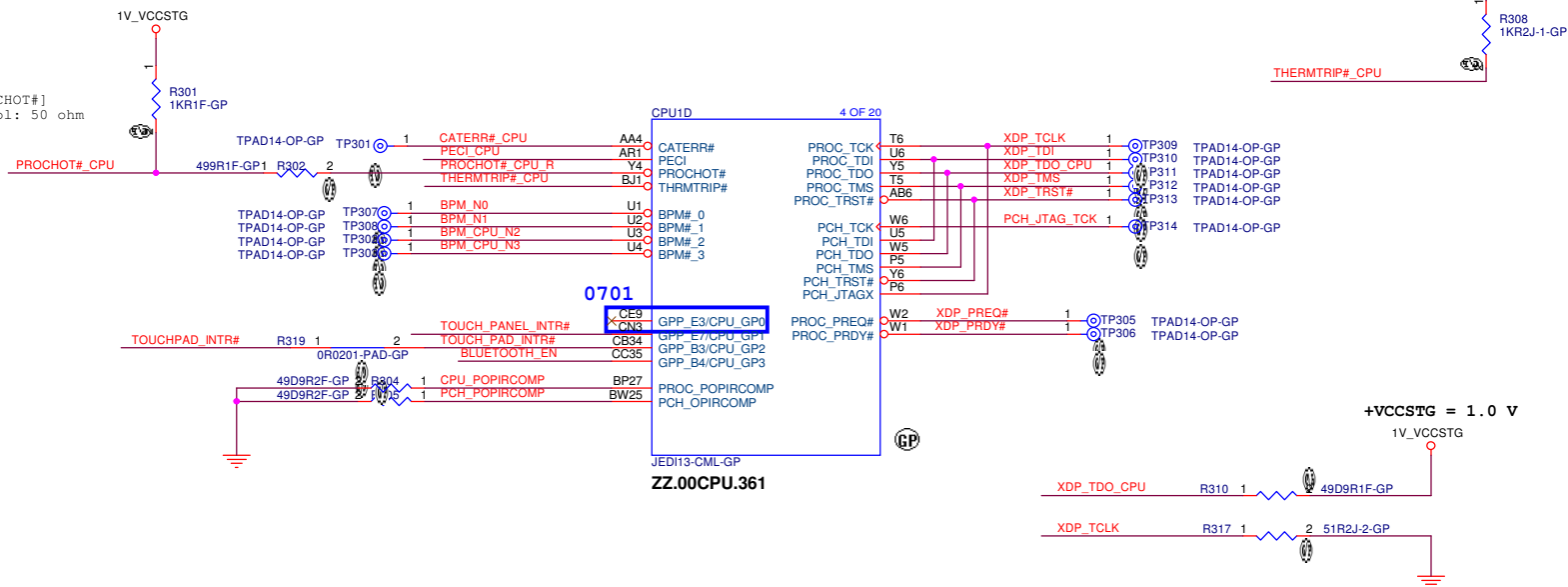


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SSID = CPU

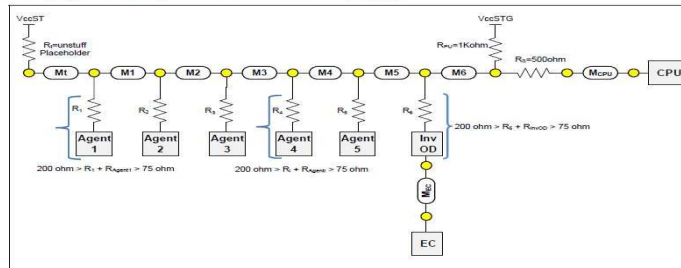
24 PECL_CPU <<>>
 24,44,46 PROCHOT#_CPU <<>>
 55 TOUCH_PANEL_INTR# <<<<
 24,65 TOUCHPAD_INTR# >>>>
 61 BLUETOOTH_EN <<<<

[PECL] and [PROCHOT#]
 Impedance control: 50 ohm



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
 M6: 1-11 inches
 MCPU: 0.3-1.5 inches
 Mt <0.3 mils
 Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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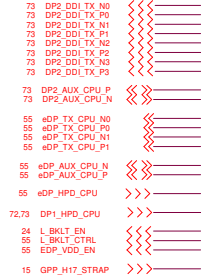
DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (THML/JTAG)			
Size A3	Document Number		Rev
		Mockingbird_CML	
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SSID = CPU

DP to HDMI2.0



DP for Type-C Mux



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

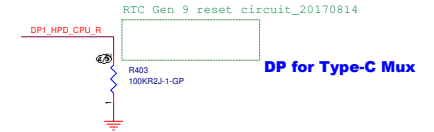
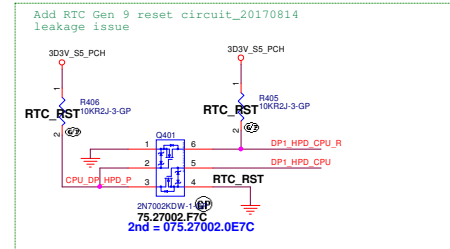
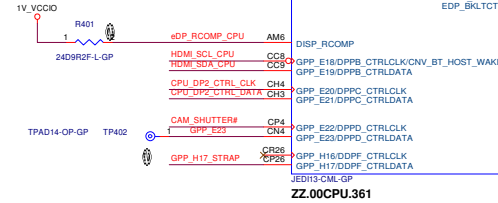
(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC

1.65GT Length 6.5" (3V1A)

DP to HDMI1.4b

DP for Type-C Mux



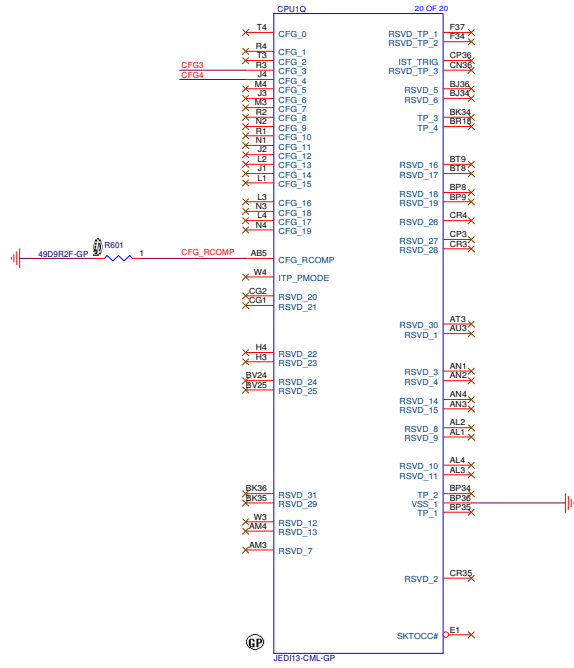
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DELL		Wistron Corporation	
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File	CPU (DDI/EDP/TBT/TPC/)		
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SSID = CPU

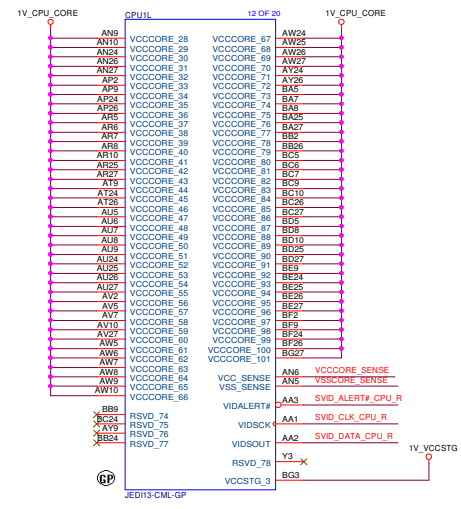
15 CFG3 <<< _____
15 CFG4 <<< _____



SKL(#543016) :
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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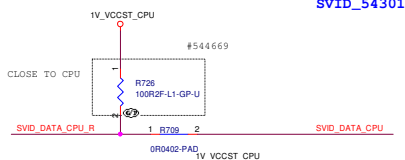
46 VCCORE_SENSE
46 VSSCORE_SENSE
46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU



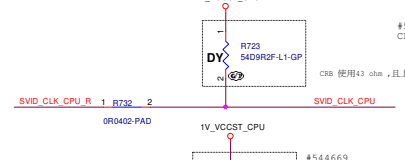
Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID_543016:

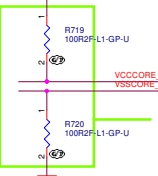
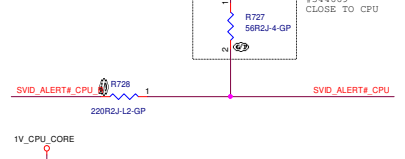
SVID DATA



SVID CLOCK



SVID ALERT



Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE
impedance=50 ohm
3. Length match<25mil

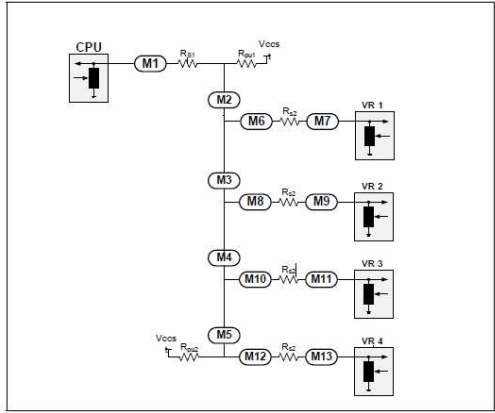
Segment	Line Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS		76	76	2992.13	2992.13

Segment	Line Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381	432	15000	17007.9
M3	MS/SL/DSL	VSS		102		4015.75	
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11

Topology Guidelines		
SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#	
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rr1=0Ω, Rr2=100Ω	
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rr1=0Ω, Rr2=49.9Ω	
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rr1=220Ω, Rr2=0Ω	
Platform resistors tolerances	± 5%	
Route ordering	When routing at minimum spacing route Alert between Data and Clock	

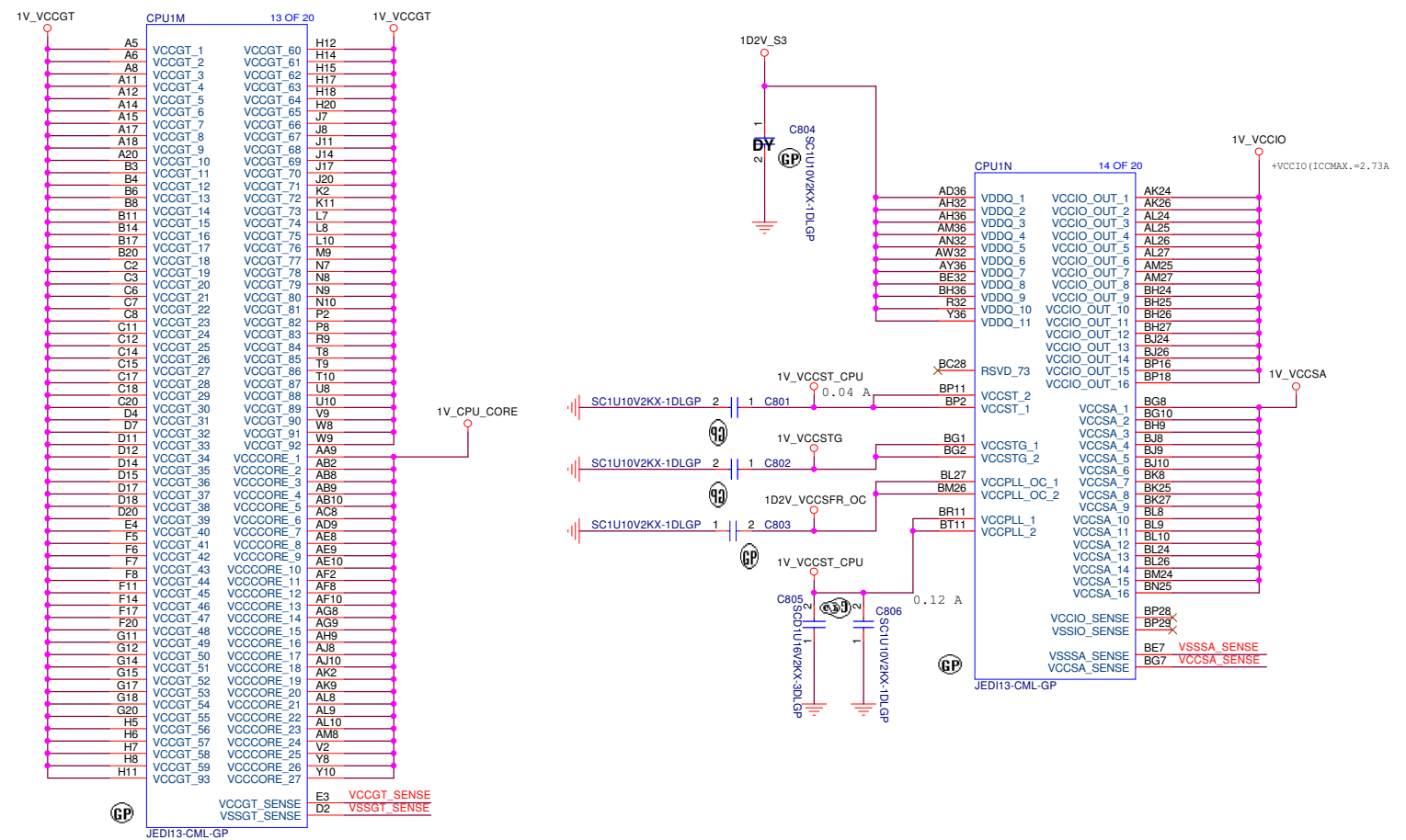
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils

Routing Illustration for SVID Topology



SSID = CPU

46 VSSSA_SENSE <<<
46 VCCSA_SENSE <<<
46 VCCGT_SENSE <<<
46 VSSGT_SENSE <<<



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DELL Wistron Corporation
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Title: **CPU (VDDQ/VCC/VCCST/VCCSTG)**

Size: A3	Document Number: Mockingbird_CML	Rev: SC
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Title

CPU (RSVD)

Size

A3

Document Number

Mockingbird_CML

Date: Monday, December 09, 2019

Rev

SC

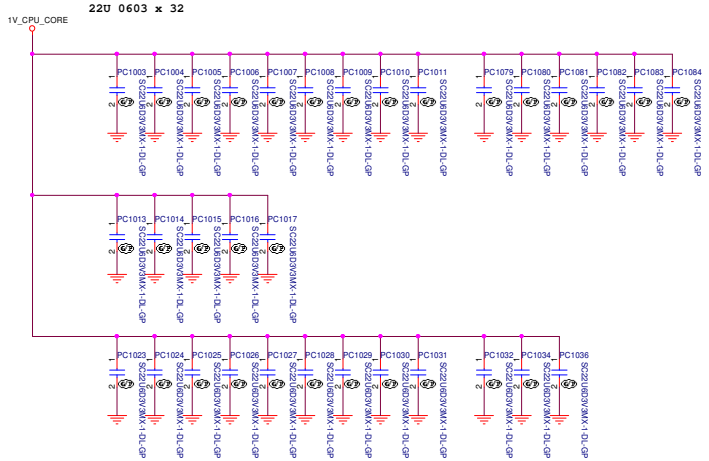
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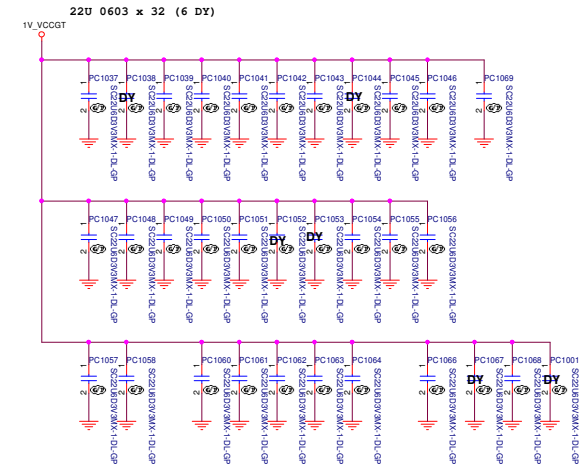
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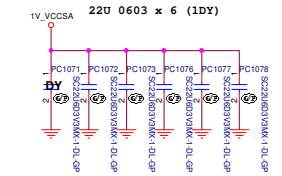
1V_CPU_CORE



VCCGT



VCCSA



Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
VCCORE Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	Place as close to the package as possible
	8x 10uF 0402		
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCGT	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
VCCSA		4x 0402	Placeholder only.
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
VDDQ			Placeholder Only
		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
VCCIO			
		6x 10uF 0402	
	4x 1uF 0201		Place underneath the package
	4x 0402		Placeholder Only
VCCPLL_OC			
	1x 1uF 0402		Do not merge VCCPLL, VCCPLL_OC and VCCGT to any noisy and high current power rail and do not route them close/adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VCCPLL			
	1x 0.1uF 0201		Place as close as possible to BGA.
		1x 1uF 0402	Place as close as possible to BGA and can be placed on as either Primary or backside cap.
		1x 0805	Placeholder Only. Can be placed on as either Primary or back side cap.
VCCGT	1x 1uF 0402		
VCCGTB	1x 1uF 0402		

Notes:

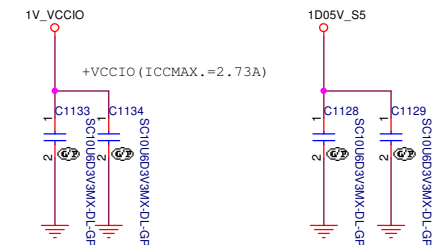
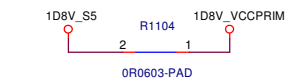
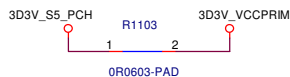
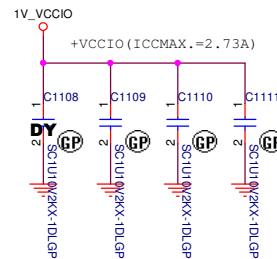
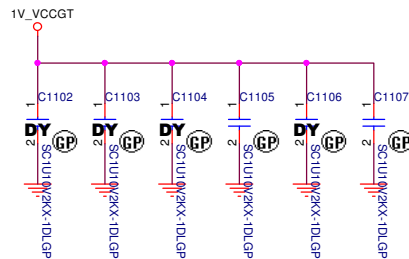
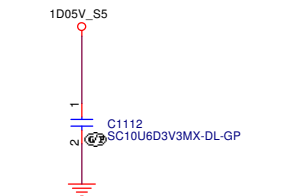
- The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR
- Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source.

SSID = CPU

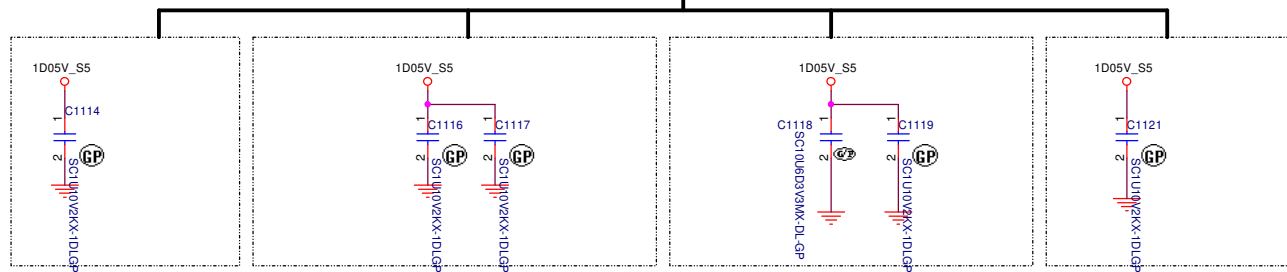
PCH DERIVED RAILS

UNSLICED GT

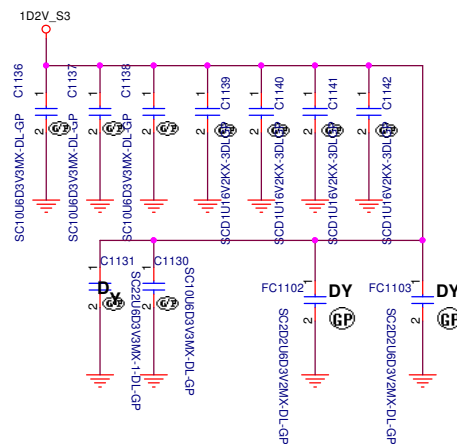
VCCIO



+VCCMPHYGTAON_1P0 (ICCMAX.=2.12A)




Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15



U-line 23e 28W
IccMax current-10ms max = 34 A

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Title			
<i>CPU (Power CAP2)</i>			
Size A3	Document Number <i>Mockingbird_CML</i>		Rev <i>SC</i>
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Title DDR (RSVD) (DDR4-CHA1)					
Size A4		Document Number Mockingbird_CML			Rev SC
Date: Monday, December 09, 2019			Sheet 14 of 105		

```
18.24.25.01 CPU_01_ROW0 <<<=====
18 CPU_000_ALERT19 <<<=====
18 CPU_000_ALERT19_00 <<<=====

18.24.25 CPU_00P_ROW0 <<<=====
18.24.25 CPU_0000_ROW0 <<<=====
20 NVR_007 <<<=====
```

```

6  CP04  <<<=====
6  CP03  <<<=====

2041  CNV_RQ_DT_R  <<<=====

18  H0A_SDOUT_CPU  >>>=====

```

Interrupt	Count	Percentage
21 GPP_K20	1	0.00%
17 INPUTDEVSEL	1	0.00%
18 CPU_SMI_ALERT#_P0	1	0.00%
21 GPP_K21	1	0.00%
21 GPE07	1	0.00%
20.25 RTC_DRSTM	1	0.00%
4 GPP_K17_STRUP	1	0.00%



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Page 8 00000 2.25 00 2.25 00



{SEN Only} PHYSICAL_DEMO_ENABLED (SPE PRIVATE)	
CPU[3]	0 - DISABLED SET SPE ENABLED BIT IN DEMO INTERFACE REG 1 - ENABLED

PCH strap pin:

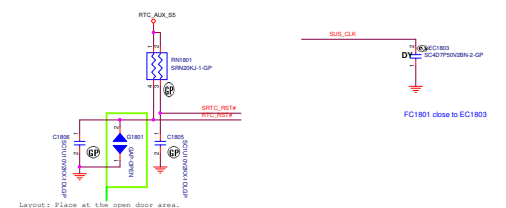
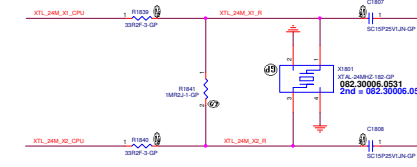
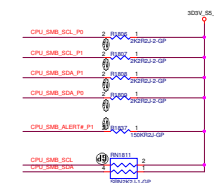
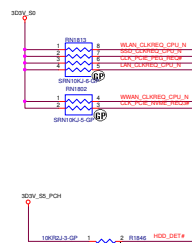


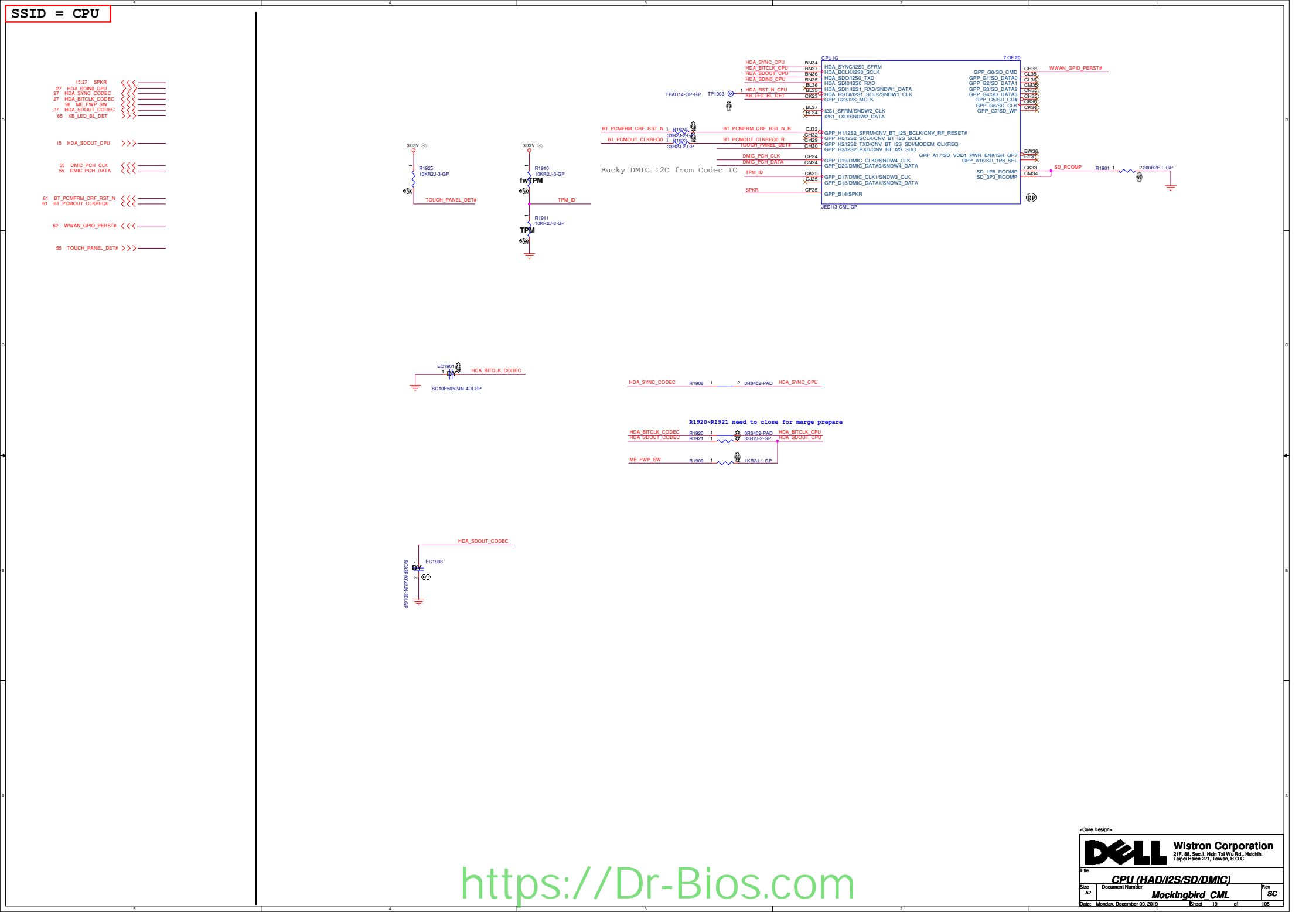
```

(00000000)
DISPLAY PORT FREQUENCY STRAP
CFO[0]
    1 -> Success
    In External Display Port device is connected to the Extended Display Port.
    0 -> Invalid device!
    In Physical Display Port attached to Extended DisplayPort". So connect for disable.

```

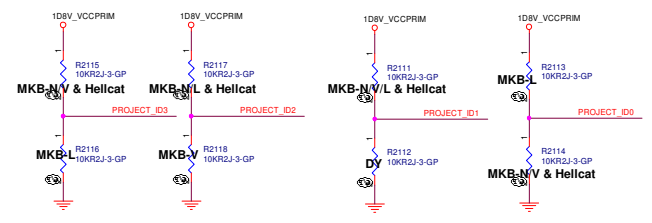
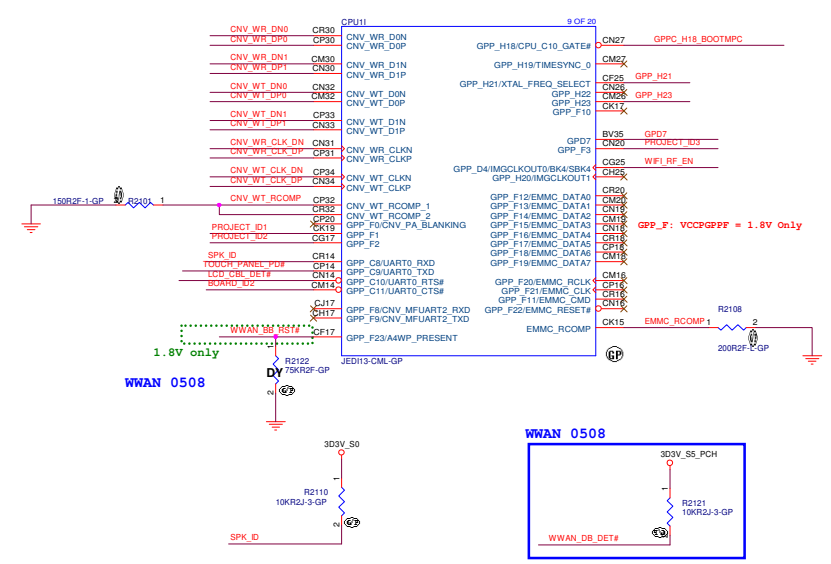






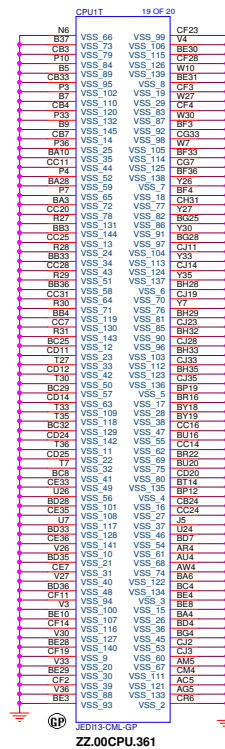
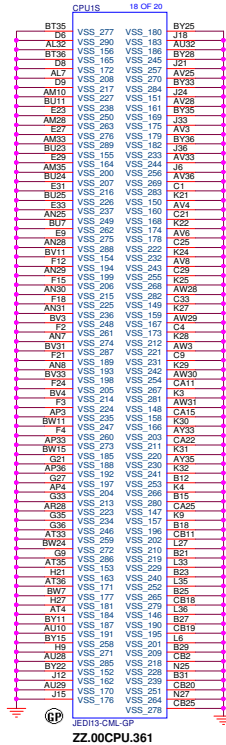
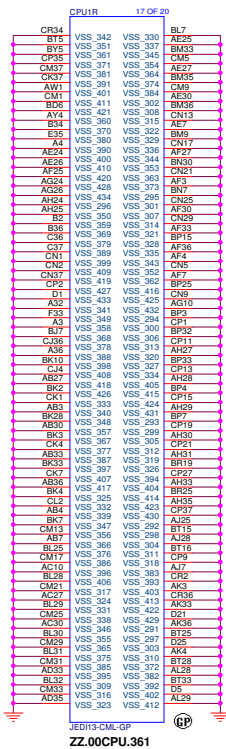
SSID = CPU

- 40 GPPC_H18_BOOTMPC <<<
- 61 WIFI_RF_EN <<<
- 55 TOUCH_PANEL_PD# <<<
- 20 BOARD_ID2 <<<
- 15 GPP_H23 >>>
- 15 GPP_H21 <<<
- 61 CNV_WT_CLK_DN >>>
- 61 CNV_WT_CLK_DP >>>
- 61 CNV_WT_DP0 >>>
- 61 CNV_WT_DN1 >>>
- 61 CNV_WT_DP1 >>>
- 61 CNV_WT_DN1 >>>
- 61 CNV_WR_CLK_DN >>>
- 61 CNV_WR_CLK_DP >>>
- 61 CNV_WR_DP0 >>>
- 61 CNV_WR_DN0 >>>
- 61 CNV_WR_DP1 >>>
- 61 CNV_WR_DN1 >>>
- 18 PROJECT_ID0 <<<
- 15 GPD7 <<<
- 62 WWAN_BB_RST# <<<
- 20.62 WWAN_DB_DET# >>>
- 20.55 LCD_CBL_DET# >>>
- 29 SPK_ID >>>



PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude (Reseved)
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Sereis
		10	5000 Series
		01	7000 Series
		00	N/A

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Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

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PCH (VSS)
Mockingbird_CML

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Size A2
Document Number
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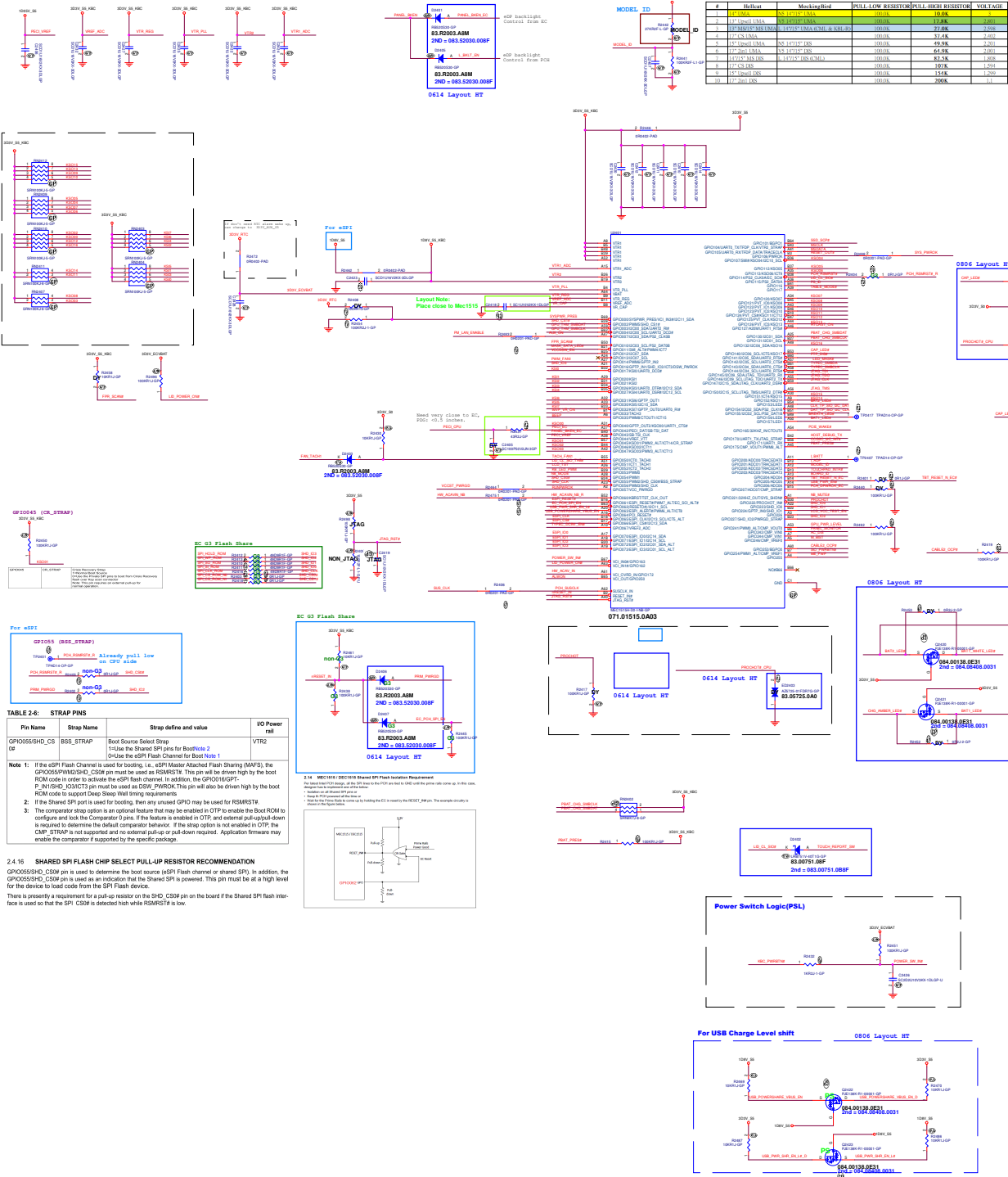
[illegible]

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPI0CS5SHD_CS3	BSS_STRAP	Boot Source Select Strap +Use the Shared SPI pins for Boot#0/1 +Use the Shared SPI Straps for Boot#1	VTRZ
<p>Note 1: If the eSPIRn Flash Strap is used for booting, i.e., as eSPIRMaster Attached Strap (MASTR), the GPI0CS5SHD_CS3 pin must be used as RBSRSTRAP. This pin will be driven high by the boot ROM code in order to activate the eSPIRn flash chip in the boot configuration. The GPIO0_CFG1.PIN1SHD_CS3CT3 pin must be used as DSW_PWVRK. This pin will also be driven high by the boot ROM code to select Deep Sleep WdgMw. Required.</p> <p>Note 2: Shared SPI port for booting for GPD can be enabled for RBSRSTRAP.</p> <p>Note 3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 2 chips. If the feature is enabled in OTP, and external pull-up/down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the boot ROM code is not supported without pull-down resistor pull down required. Application firmware may enable the comparator if supported by the specific package.</p>			

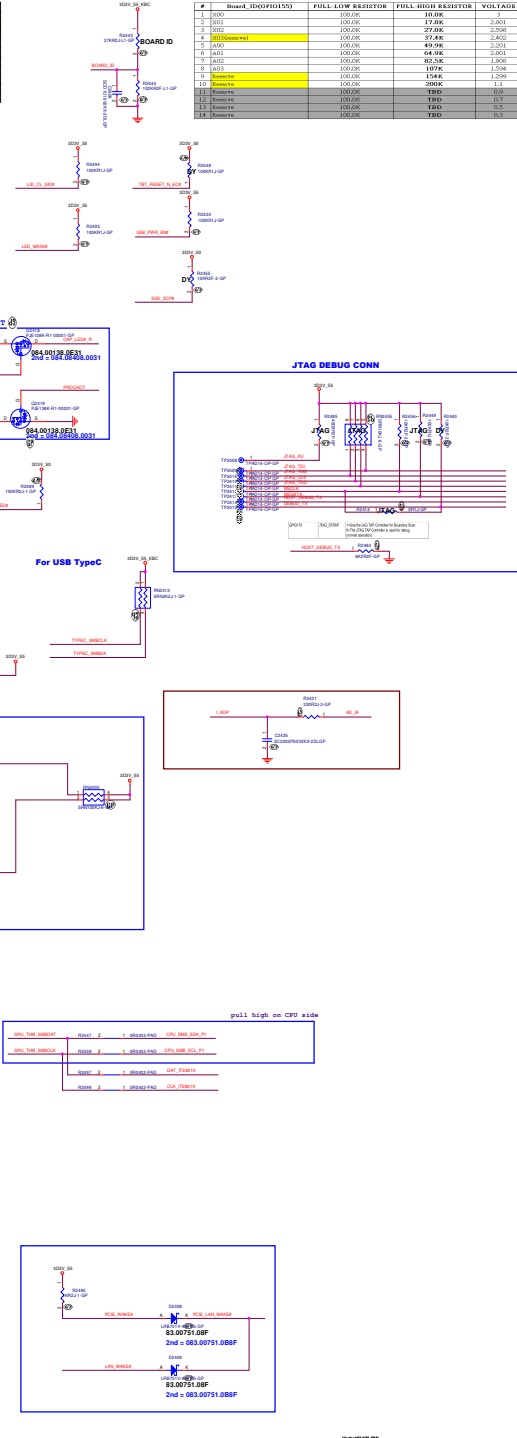
2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI_CS0# is detected high while RSMRST# is low.



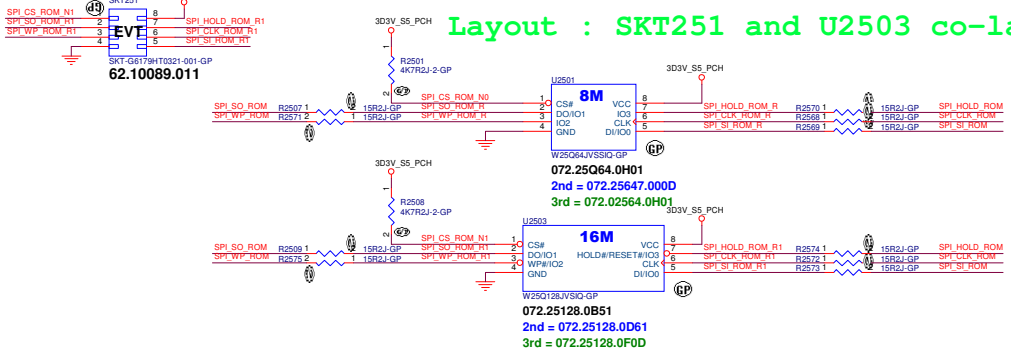
BOARD ID		Board: Hecopip1550	FULL LOW RESISTOR	FULL HIGH RESISTOR	VOLTAGE
BOARD ID	1	1000	100.0%	17.8%	29.8
	2	1000	100.0%	17.8%	29.8
	3	1000	100.0%	17.8%	29.8
	4	1000	100.0%	17.8%	29.8
	5	1000	100.0%	17.8%	29.8
	6	1000	100.0%	17.8%	29.8
	7	1000	100.0%	17.8%	29.8
	8	1000	100.0%	17.8%	29.8
	9	1000	100.0%	17.8%	29.8
	10	1000	100.0%	17.8%	29.8
BOARD ID	11	1000	100.0%	17.8%	29.8
	12	1000	100.0%	17.8%	29.8
	13	1000	100.0%	17.8%	29.8
	14	1000	100.0%	17.8%	29.8
	15	1000	100.0%	17.8%	29.8
	16	1000	100.0%	17.8%	29.8
	17	1000	100.0%	17.8%	29.8
	18	1000	100.0%	17.8%	29.8
	19	1000	100.0%	17.8%	29.8
	20	1000	100.0%	17.8%	29.8
BOARD ID	21	1000	100.0%	17.8%	29.8
	22	1000	100.0%	17.8%	29.8
	23	1000	100.0%	17.8%	29.8
	24	1000	100.0%	17.8%	29.8
	25	1000	100.0%	17.8%	29.8
	26	1000	100.0%	17.8%	29.8
	27	1000	100.0%	17.8%	29.8
	28	1000	100.0%	17.8%	29.8
	29	1000	100.0%	17.8%	29.8
	30	1000	100.0%	17.8%	29.8
BOARD ID	31	1000	100.0%	17.8%	29.8
	32	1000	100.0%	17.8%	29.8
	33	1000	100.0%	17.8%	29.8
	34	1000	100.0%	17.8%	29.8
	35	1000	100.0%	17.8%	29.8
	36	1000	100.0%	17.8%	29.8
	37	1000	100.0%	17.8%	29.8
	38	1000	100.0%	17.8%	29.8
	39	1000	100.0%	17.8%	29.8
	40	1000	100.0%	17.8%	29.8
BOARD ID	41	1000	100.0%	17.8%	29.8
	42	1000	100.0%	17.8%	29.8
	43	1000	100.0%	17.8%	29.8
	44	1000	100.0%	17.8%	29.8
	45	1000	100.0%	17.8%	29.8
	46	1000	100.0%	17.8%	29.8
	47	1000	100.0%	17.8%	29.8
	48	1000	100.0%	17.8%	29.8
	49	1000	100.0%	17.8%	29.8
	50	1000	100.0%	17.8%	29.8
BOARD ID	51	1000	100.0%	17.8%	29.8
	52	1000	100.0%	17.8%	29.8
	53	1000	100.0%	17.8%	29.8
	54	1000	100.0%	17.8%	29.8
	55	1000	100.0%	17.8%	29.8
	56	1000	100.0%	17.8%	29.8
	57	1000	100.0%	17.8%	29.8
	58	1000	100.0%	17.8%	29.8
	59	1000	100.0%	17.8%	29.8
	60	1000	100.0%	17.8%	29.8



SSID = SPI Flash

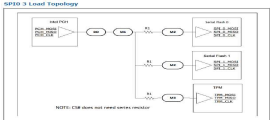
18,24 SPI_CS_ROM_N1 >>>
18,24 SPI_CS_ROM_N0 >>>
18,24,91 SPI_SO_ROM <<<
18,24,91 SPI_CLK_ROM >>>
15,18,24,91 SPI_SI_ROM >>>
15,18,24 SPI_HOLD_ROM <<<
15,18,24 SPI_WP_ROM <<<

Socket for 16M



Dual SPI0 Devices + TPM Topology Guidelines

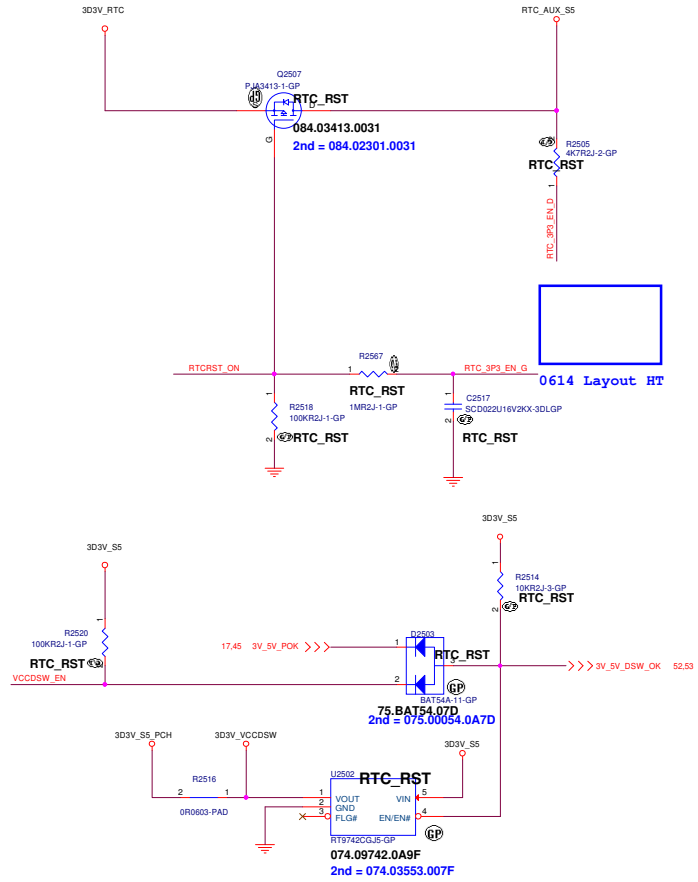
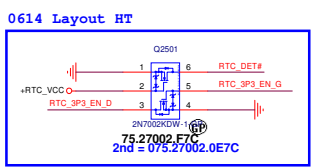
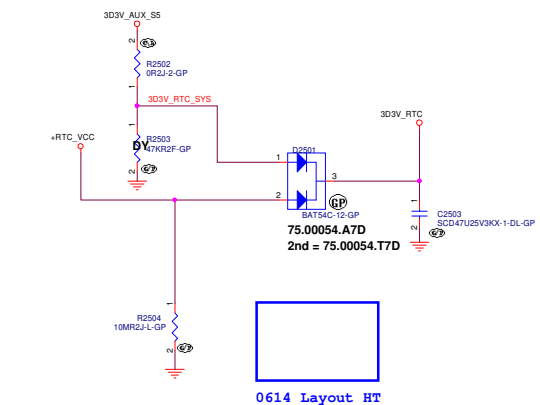
The CFL PCH supports TPM through SPI0 bus. The topology below was a full configuration which consist of 2 SPI0 Flash and 1 TPM device. The system can be configured with 1 SPI0 Flash and 1 TPM device.



Segment	Time Type	Reference	Via Count	Max Length, mm		Max Length, mils	
				Segment	Total	Segment	Total
Notes:							
R1 Resistor should be 15 ohm for 1.8V and 33 ohm for 3.3V. SPI0_I/O2 and SPI0_I/O3 connection to be pulled up with 1k ohm on R2 resistor.							
5 number of via can be allowed.							
Reference plane should be Continuous Ground Plane only allowed.							
This topology relates to SPI0_I/O2 to 3, SPI0_MOSI, SPI0_MISO and SPI0_CLK							
Design guideline support up to 50MHz.							

SSID = RTC

15,20 RTC_DET# <<<
24 VCCDSW_EN >>>
24 RTCRST_ON >>>



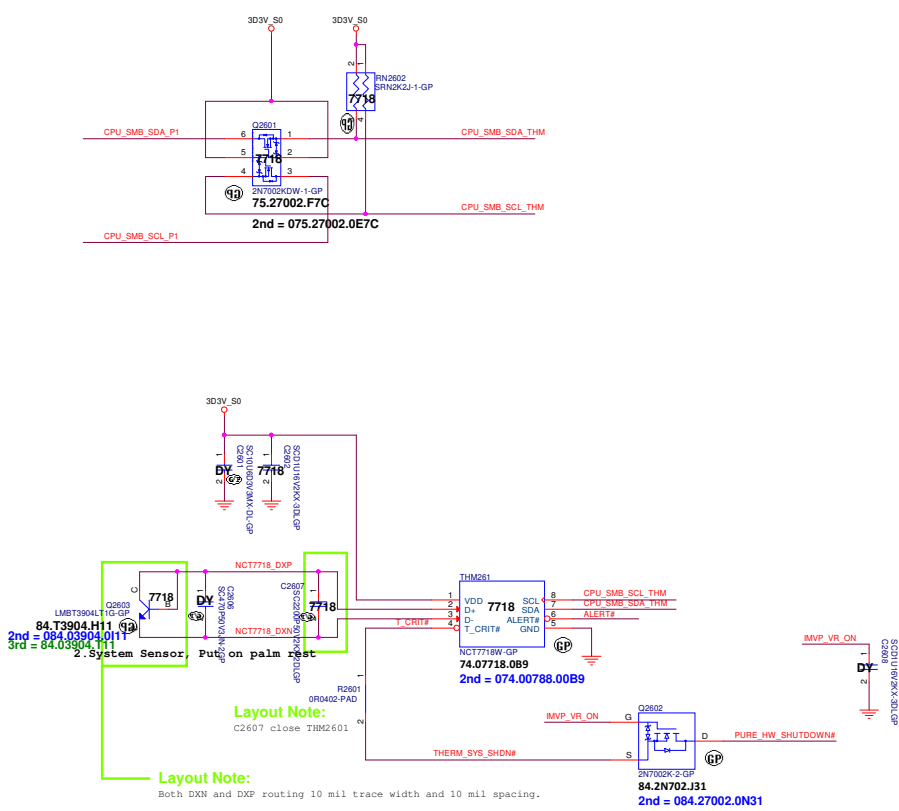
<https://Dr-Bios.com>

SSID = Thermal Sensor

18.24 CPU_SMB_SDA_P1 <<>>
18.24 CPU_SMB_SCL_P1 <<>>

17.24 MVP_VR_ON >>>>
40 PURE_HW_SHUTDOWN# <<<<

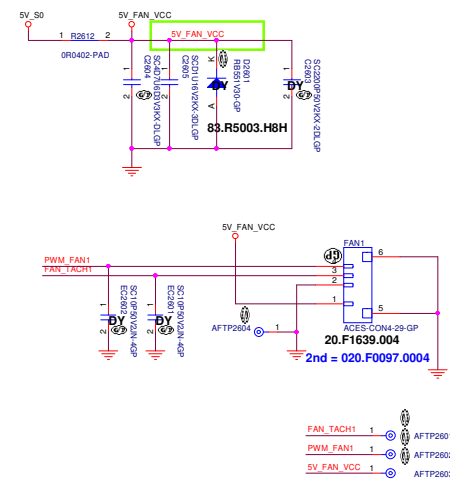
24 PWM_FAN1 >>>>
24 FAN_TACH1 <<<<



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1

Layout Note:
Signal Routing Guideline:
Trace width = 15mil



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SSID = Audio

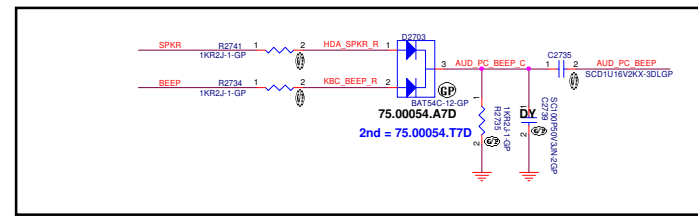
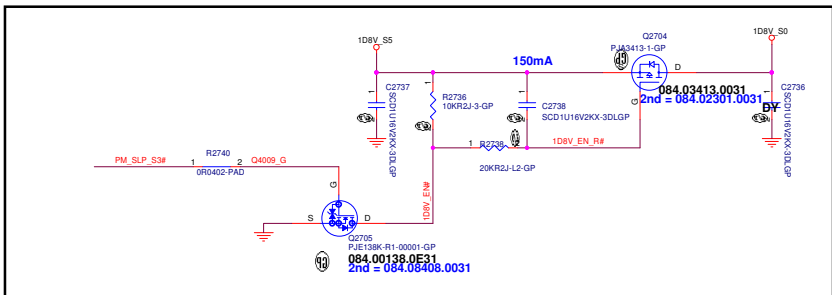
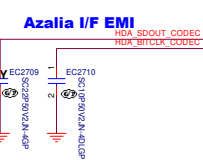
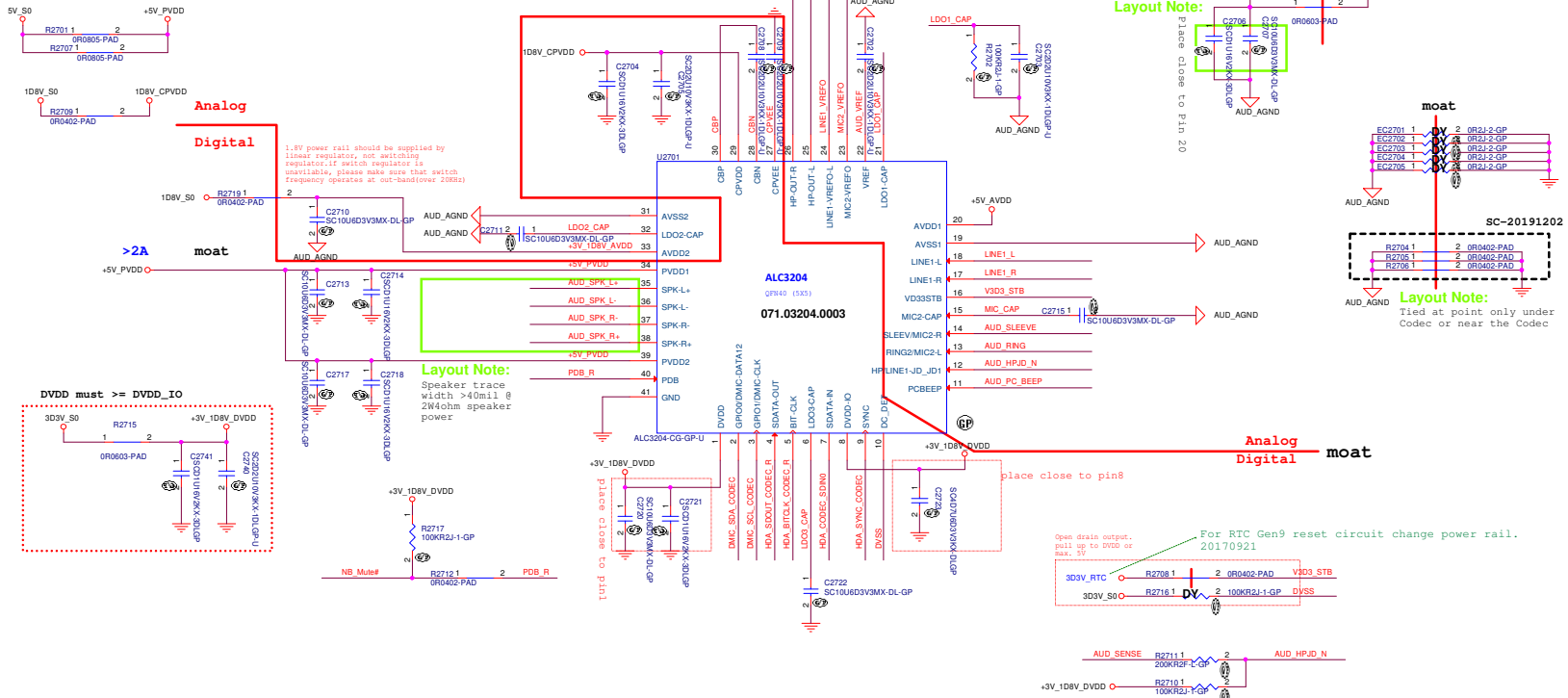
19 HDA_SDIN0_CPU <<<
19 HDA_SDOUT_CODEC >>>
19 HDA_SYNC_CODEC >>>
19 HDA_BITCLK_CODEC >>>

29 AUD_SPK_R <<<
29 AUD_SPK_L <<<
29 AUD_SPK_L+ <<<
29 AUD_SPK_L- <<<

24 NB_Mute# >>>
15,19 SPKR >>>
24 BEEP >>>
66 AUD_SENSE >>>
29 LINE1_VREF0 <<<
29 MIC2_VREF0 <<<
29 AUD_HP1_JACK_L <<<
29 AUD_HP1_JACK_R <<<
29 LINE1_L >>>
29 LINE1_R >>>

28,66 AUD_SLEEVE <<<
29,66 AUD_RING <<<
55 DMIC_SCL_CODEC <<<
55 DMIC_SDA_CODEC <<<
17,40,55 PM_SLP_S3# >>>

Audio Codec Chip ALC3204




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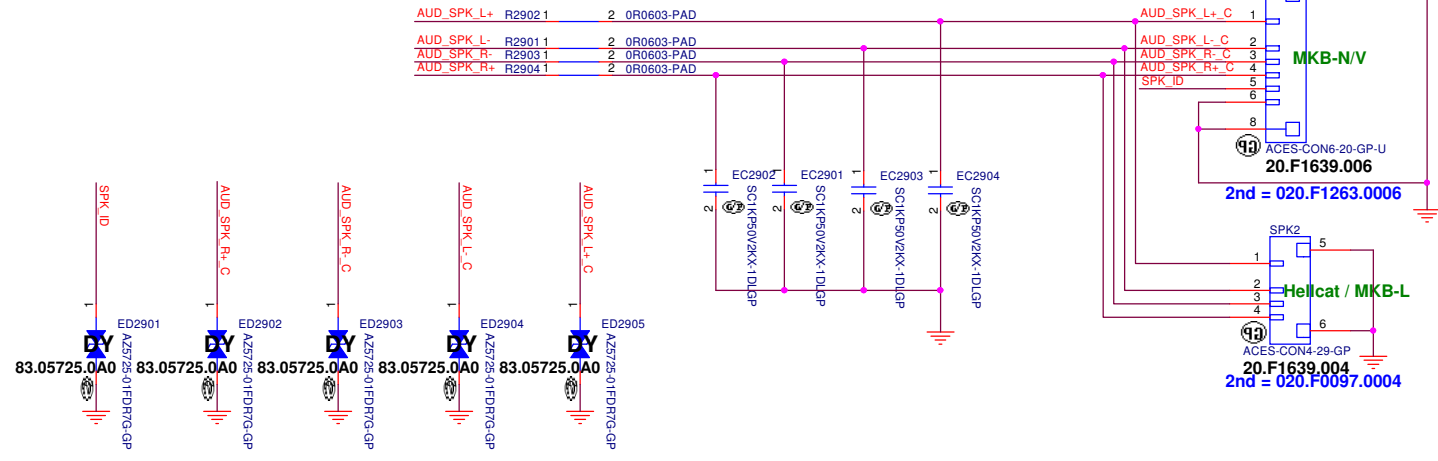
SSID = Audio

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

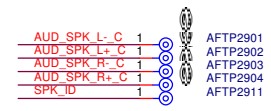
27 AUD_SPK_R+ >>>
27 AUD_SPK_R- >>>
27 AUD_SPK_L- >>>
27 AUD_SPK_L+ >>>

21 SPK_ID <<<



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

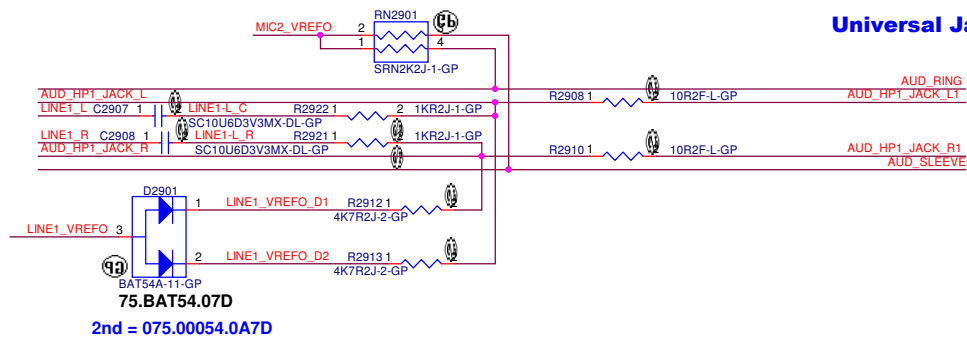
SPK_ID 1: FG
0: Veci



From Codec

27 MIC2_VREFO >>>
27,29,66 AUD_RING <<<
27 AUD_HP1_JACK_L >>>
27 LINE1_L >>>
27 LINE1_R >>>

27 AUD_HP1_JACK_R >>>
27,29,66 AUD_SLEEVE <<<
27 LINE1_VREFO >>>



Universal Jack (Moved to I/O Board)

To IO Board

27,29,66 AUD_RING <<<
66 AUD_HP1_JACK_L1 <<<
66 AUD_HP1_JACK_R1 <<<
27,29,66 AUD_SLEEVE <<<

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Title **Audio IO**


Size A3 Document Number **Mockingbird CML** Rev **SC**

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Title		
LAN RTL8106		
Size	Document Number	Rev
Custom	Mockingbird CML	SC
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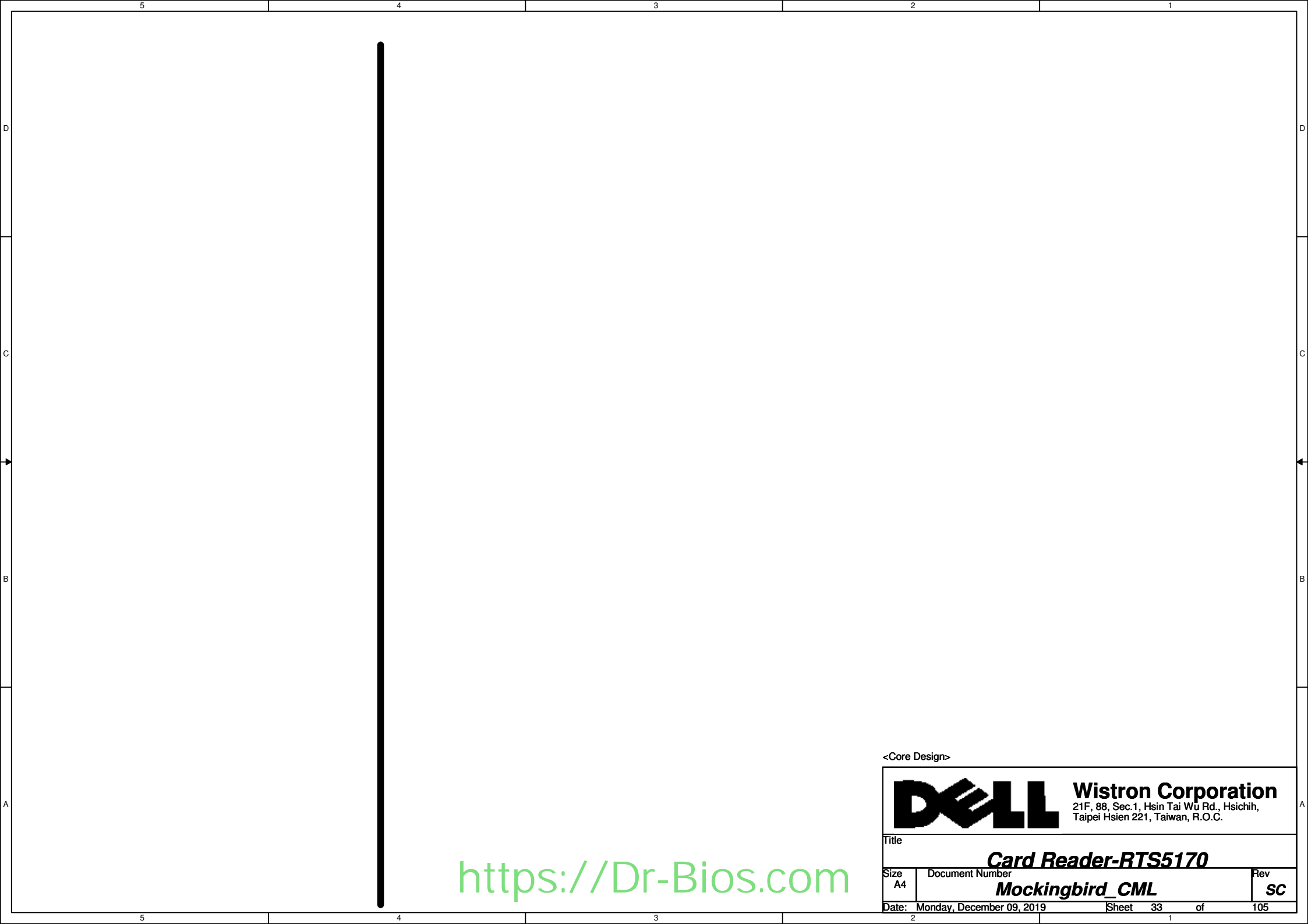


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Title

XFOM&RJ45

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Title			
Card Reader-RTS5170			
Size	Document Number		Rev
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Title		
USB2.0 CONN		
Size	Document Number	Rev
	Mockingbird_CML	SC
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SSID = USB3.0 Port1

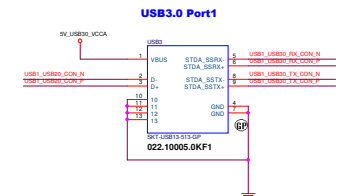
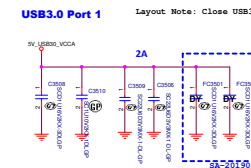
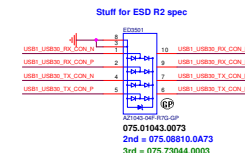
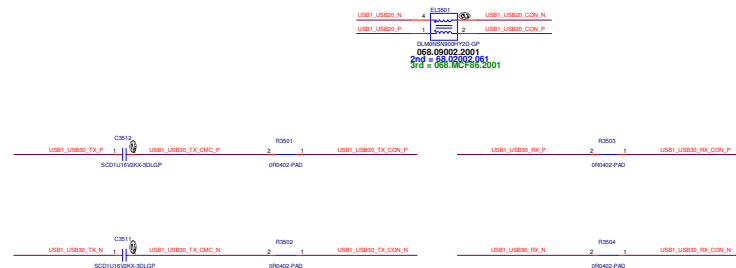
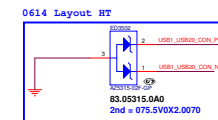
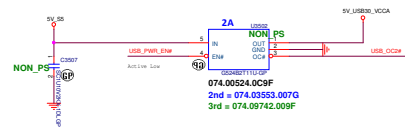
24.05 USB_PWFL_ENW <<<—
16.36 USB_OC2W <<<—

36 USB1_USB20_N <<<—
36 USB1_USB20_P <<<—

16 USB1_USB20_TX_N >>>—
16 USB1_USB20_TX_P >>>—
16 USB1_USB20_RX_N >>>—
16 USB1_USB20_RX_P >>>—

Main Func = USB3.0 Port2

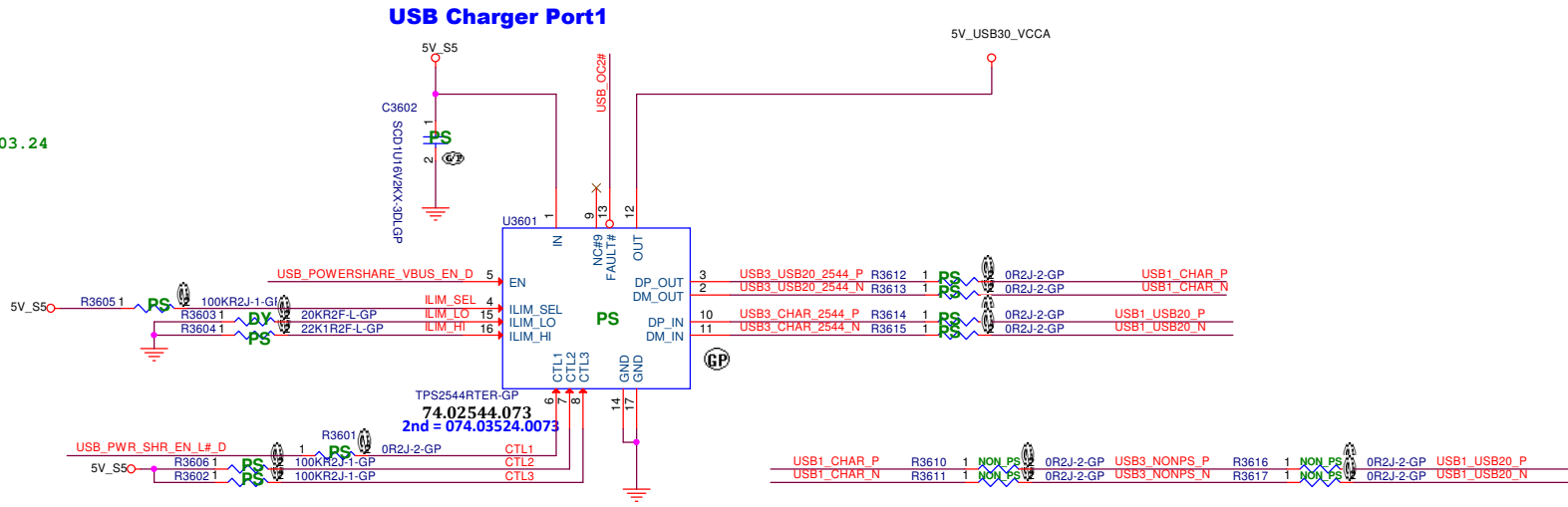
0513



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SSID = USB Charger

2018.03.24




Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS_VP} (mA) = \frac{50,500}{(R_{ILIM_XX} (k\Omega) + 0.1)}$$

R_{ILIM,XX} corresponds to either R_{ILIM,HI} or R_{ILIM,LO} as appropriate.

BOLT 15 32bit 0822




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Title			USB Charger	
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Title			
USB3.0 PORT			
Size A4	Document Number Mockingbird_CML		Rev SC
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Title			
<i>Reserved</i>			
Size A4	Document Number <i>Mockingbird_CML</i>		Rev <i>SC</i>
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Title		
(RSVD)		
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D

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C

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B

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A

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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684

Connected_Standby(1/2)+DS3

Size

A4

Document Number

Mockingbird CML

Rev

SC


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Title Connected_Standby(2/2)			
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ISL9538C For Charger

OFFPAGE

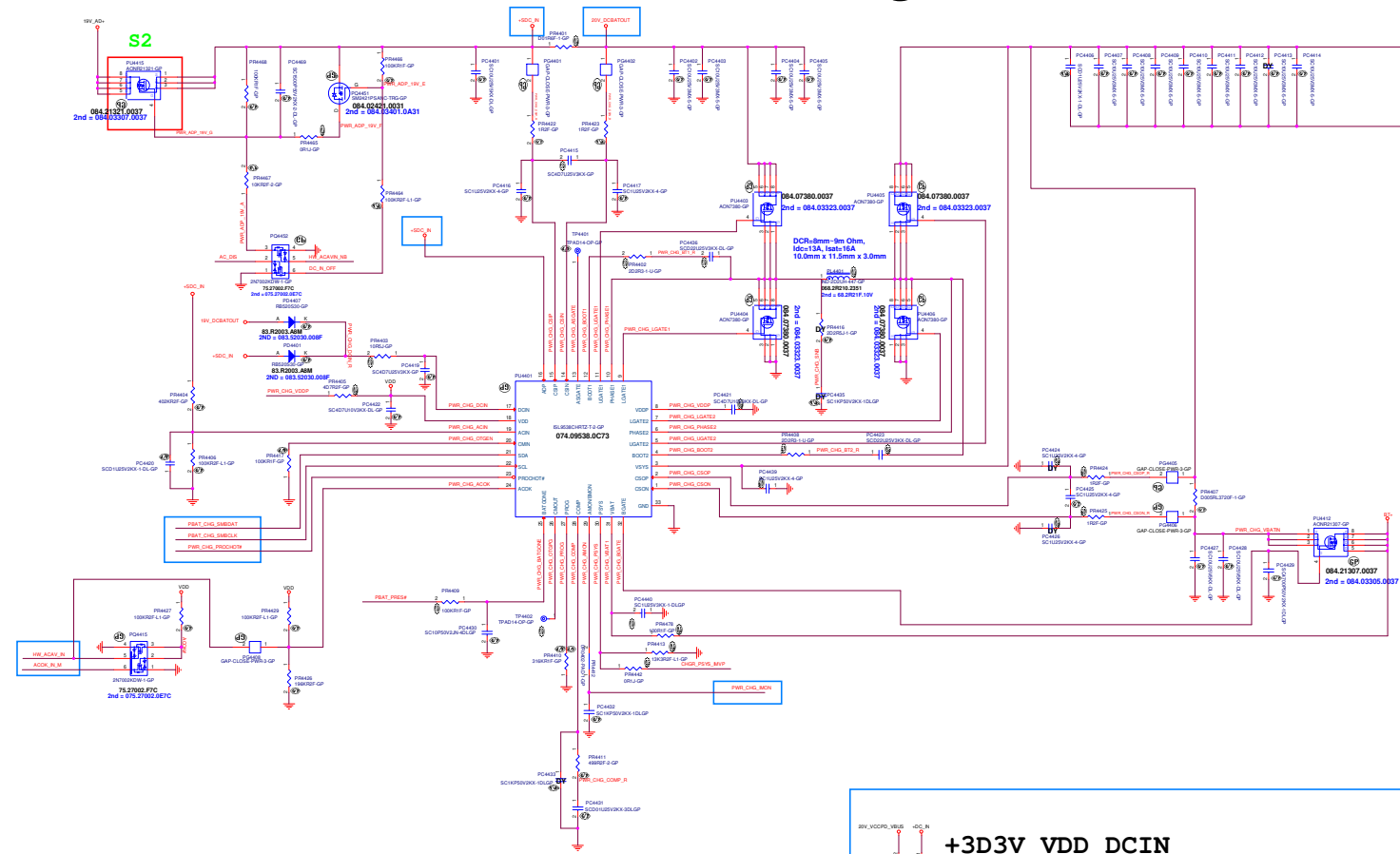
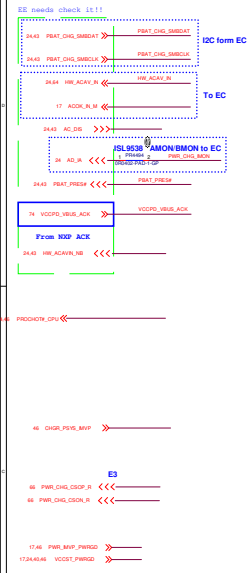
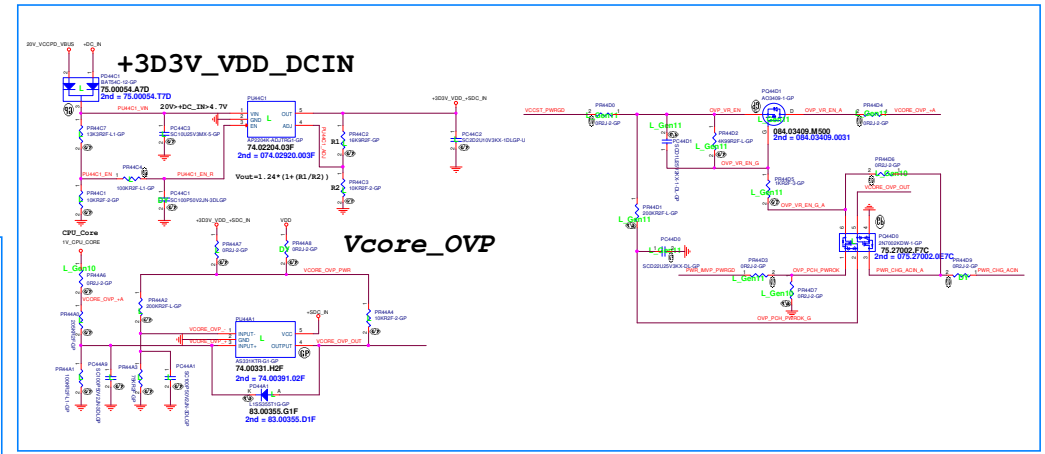
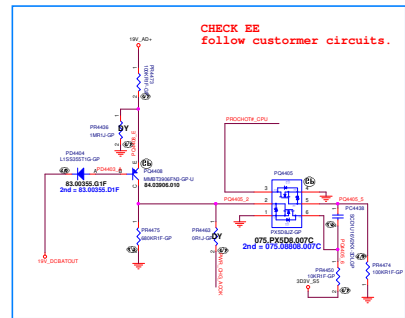
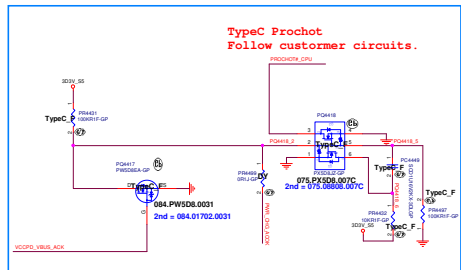
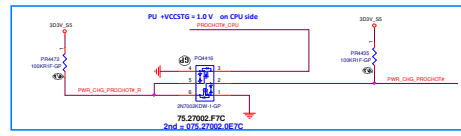


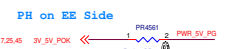
TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-AND RESISTANCE (Ω)	MIN	1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT AC2inMS Reg(A)
0	8.45	14.7	21.0	1	733kHz	No	0.476
8.45	14.7	21.0	28.0	2	733kHz	No	1.5
14.7	21.0	28.0	35.7	3	733kHz	Yes	0.476
21.0	28.0	35.7	43.2	4	733kHz	Yes	1.5
28.0	35.7	43.2	50.5	5	733kHz	Yes	0.476
35.7	43.2	50.5	58.0	6	733kHz	Yes	1.5
43.2	50.5	58.0	60.5	7	733kHz	Yes	0.476
50.5	58.0	60.5	63.0	8	733kHz	Yes	1.5
58.0	60.5	63.0	65.5	9	733kHz	Yes	0.476
60.5	63.0	65.5	68.0	10	733kHz	Yes	1.5
63.0	65.5	68.0	70.5	11	733kHz	Yes	0.476
65.5	68.0	70.5	73.0	12	733kHz	Yes	1.5
68.0	70.5	73.0	75.5	13	733kHz	Yes	0.476
70.5	73.0	75.5	78.0	14	733kHz	Yes	1.5
73.0	75.5	78.0	80.5	15	733kHz	Yes	0.476
75.5	78.0	80.5	83.0	16	733kHz	Yes	1.5
78.0	80.5	83.0	85.5	17	733kHz	Yes	0.476
80.5	83.0	85.5	88.0	18	733kHz	Yes	1.5
83.0	85.5	88.0	90.5	19	733kHz	Yes	0.476
85.5	88.0	90.5	93.0	20	733kHz	Yes	1.5
88.0	90.5	93.0	95.5	21	733kHz	Yes	0.476
90.5	93.0	95.5	98.0	22	733kHz	Yes	1.5
93.0	95.5	98.0	100.5	23	733kHz	Yes	0.476
95.5	98.0	100.5	103.0	24	733kHz	Yes	1.5
98.0	100.5	103.0	105.5	25	733kHz	Yes	0.476
100.5	103.0	105.5	108.0	26	733kHz	Yes	1.5
103.0	105.5	108.0	110.5	27	733kHz	Yes	0.476
105.5	108.0	110.5	113.0	28	733kHz	Yes	1.5
108.0	110.5	113.0	115.5	29	733kHz	Yes	0.476
110.5	113.0	115.5	118.0	30	733kHz	Yes	1.5
113.0	115.5	118.0	120.5	31	733kHz	Yes	0.476
115.5	118.0	120.5	123.0	32	733kHz	Yes	1.5
118.0	120.5	123.0	125.5	33	733kHz	Yes	0.476
120.5	123.0	125.5	128.0	34	733kHz	Yes	1.5



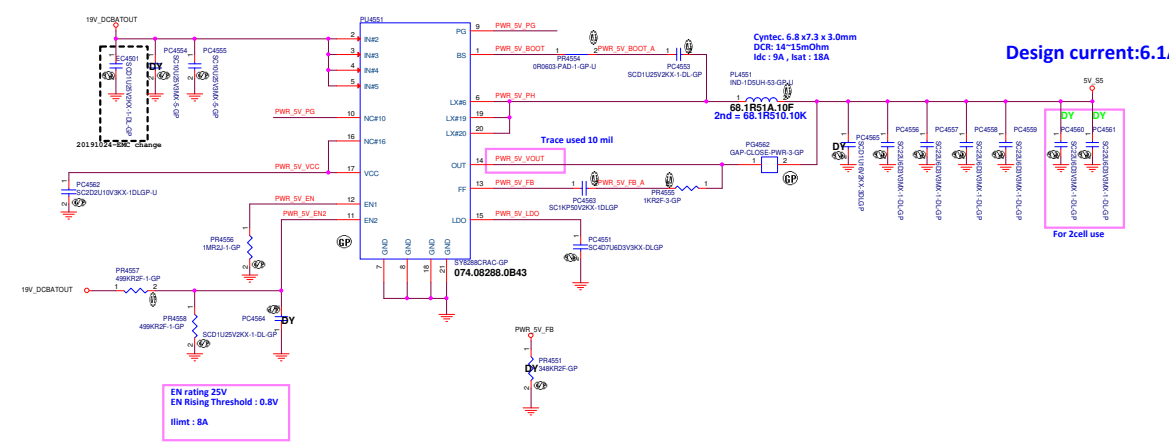
SSID = PWR.Plane.Regulator_5V

OFFPAGE-Signal



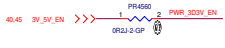
OFFPAGE-GAP

SY8288C For 5V

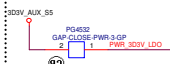


SSID = PWR.Plane.Regulator_3D3V

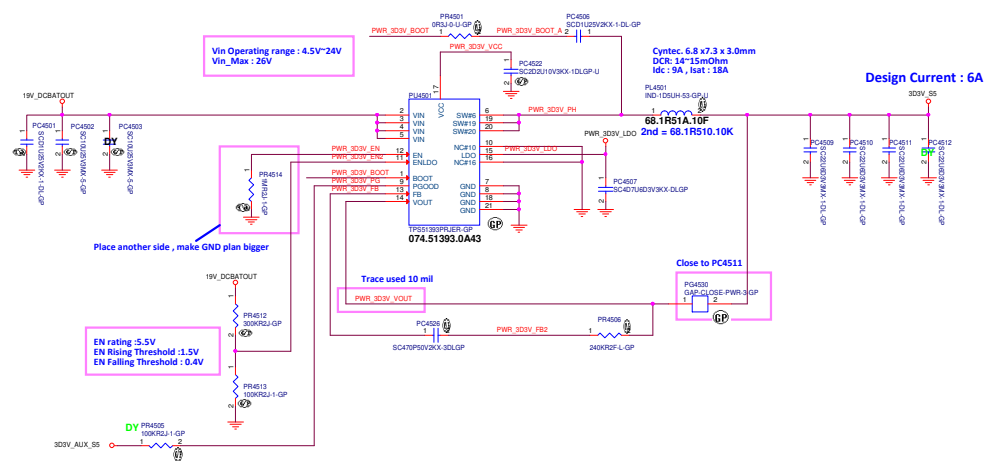
OFFPAGE-Signal



OFFPAGE-GAP



TPS51393 For 3D3V



<https://Dr-Bios.com>

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POWER (8288_5V/51393_3D3V)

Doc No: Mockingbird_CML

Date: Monday, December 18, 2018

Rev	Doc No	Rev
1	1	1

PH on CPU side

32444 PROCHOTX_CPU <<<—
 7 SVID_ALERTX_CPU <<<—
 7 SVID_CLK_CPU >>>—
 7 SVID_DATA_CPU >>>—
 1744 PWR_BMP_PWRIGD >>>—
 17244244 VCCST_PWRIGD >>>—

For VCCGT Sense

8 VCCGT_SENSE >>>—
 8 VCCST_SENSE >>>—

For Vcore Sense

7 VCCORE_SENSE >>>—
 7 VCCORE_SENSE >>>—

For Vccsa Sense

8 VCCSA_SENSE >>>—
 8 VCCSA_SENSE >>>—

EE side Link

SVID Pull High V

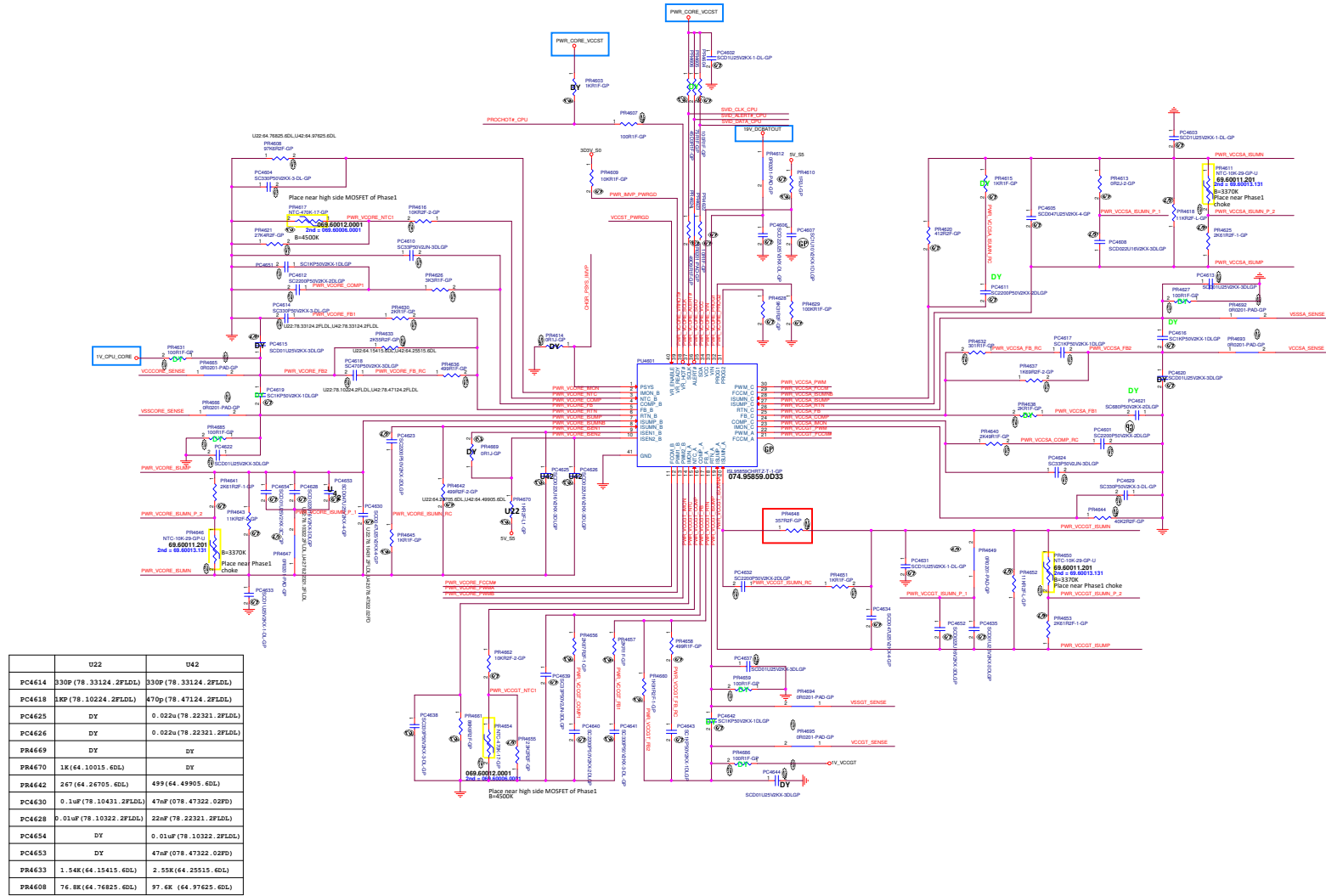
TV_VCCST_CPU >>>—
 PWR_CORE_VCCST >>>—

47 PWR_VCORE_PMA8 >>>—
 47 PWR_VCORE_S0A0 >>>—
 47 PWR_VCORE_S0A0 >>>—
 47 PWR_VCORE_F0C0 >>>—
 47 PWR_VCORE_PMA8 >>>—
 47 PWR_VCCST_PMA8 >>>—
 48 PWR_VCCST_F0C0 >>>—
 48 PWR_VCCST_S0A0 >>>—
 48 PWR_VCCSA_S0A0 >>>—
 50 PWR_VCCSA_PMA8 >>>—
 50 PWR_VCCSA_F0C0 >>>—

47 PWR_VCORE_SEN1 >>>—
 47 PWR_VCORE_SEN2 >>>—

44 CHGR_P0Y0_BMP >>>—

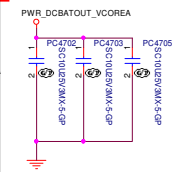
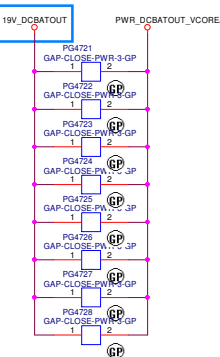
ISL95859C For CPUCORE



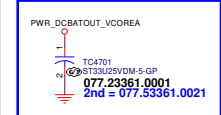
<https://Dr-Bios.com>

SSID = CPU_CORE

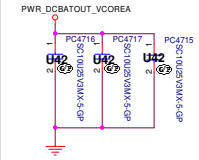
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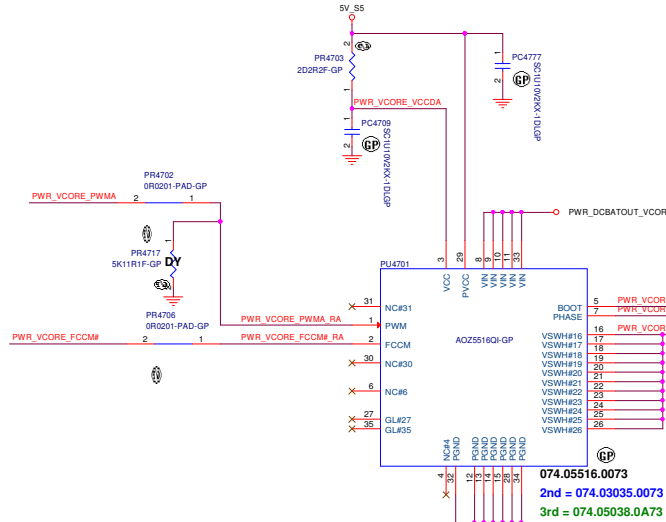
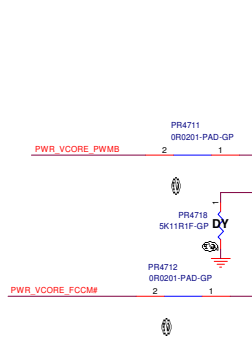
For acoustic noise



- 46 PWR_VCORE_PWM_A
- 46.47 PWR_VCORE_FCCM
- 46.47 PWR_VCORE_ISEN1
- 46.47 PWR_VCORE_ISUMP
- 46.47 PWR_VCORE_ISUMN
- 46.47 PWR_VCORE_ISEN2



- 46 PWR_VCORE_PWM_B
- 46.47 PWR_VCORE_FCCM
- 46.47 PWR_VCORE_ISEN2
- 46.47 PWR_VCORE_ISUMP
- 46.47 PWR_VCORE_ISUMN
- 46.47 PWR_VCORE_ISEN1



074.05516.0073
2nd = 074.03035.0073
3rd = 074.05038.0A73

<https://Dr-Bios.com>

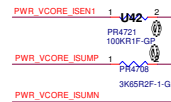
KBL-R_U42_15W
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 37A , Isat : 41A

068.R1510.2041
2nd = 068.R1510.1141

PT4701
SE330U2VDM-4-GP
79.33719.20C
2nd = 80.3371V.L01



PWR_VCORE_ISEN1

PWR_VCORE_ISUMP

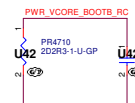
PWR_VCORE_ISUMN

PWR_VCORE_ISEN2

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Idc : 37A , Isat : 41A

068.R1510.2041
2nd = 068.R1510.1141

PT4703
SE330U2VDM-4-GP
79.33719.20C
2nd = 80.3371V.L01



PWR_VCORE_BOOTB

PWR_VCORE_SWB

PWR_VCORE_ISEN2

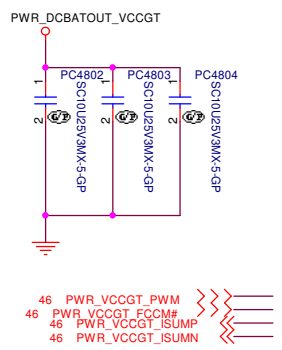
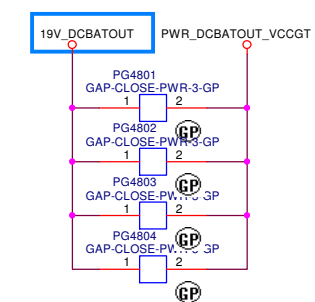
PWR_VCORE_ISUMP

PWR_VCORE_ISUMN

PWR_VCORE_ISEN1

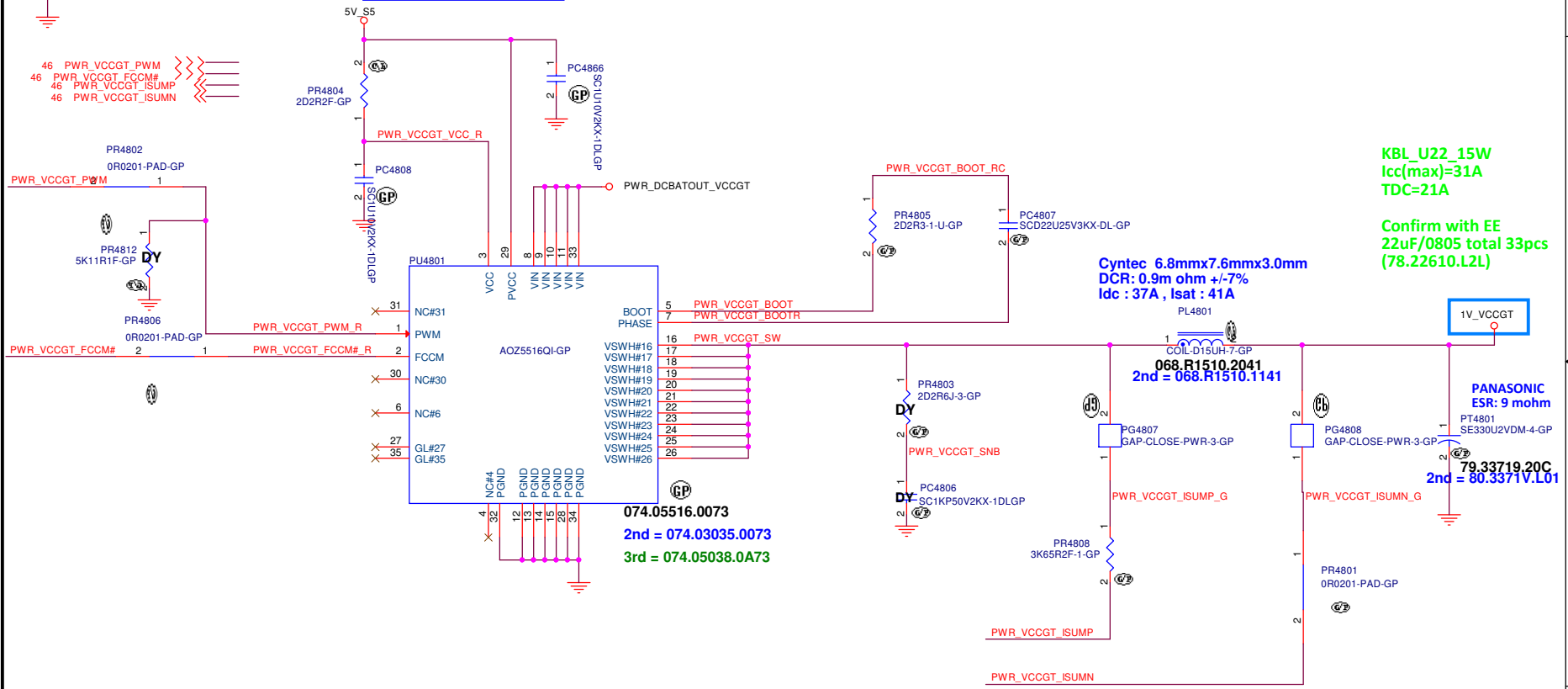
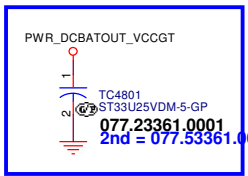
SSID = CPU_CORE

Offpage-Signal



AOZ5516Q For VCCGT

For acoustic noise



KBL_U22_15W
Icc(max)=31A
TDC=21A

Confirm with EE
22uF/0805 total 33pcs
(78.22610.L2L)

Cyntec 6.8mmx7.6mmx3.0mm
DCR: 0.9m ohm +/-7%
Isc : 37A , Isat : 41A

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RSVD

<https://Dr-Bios.com>

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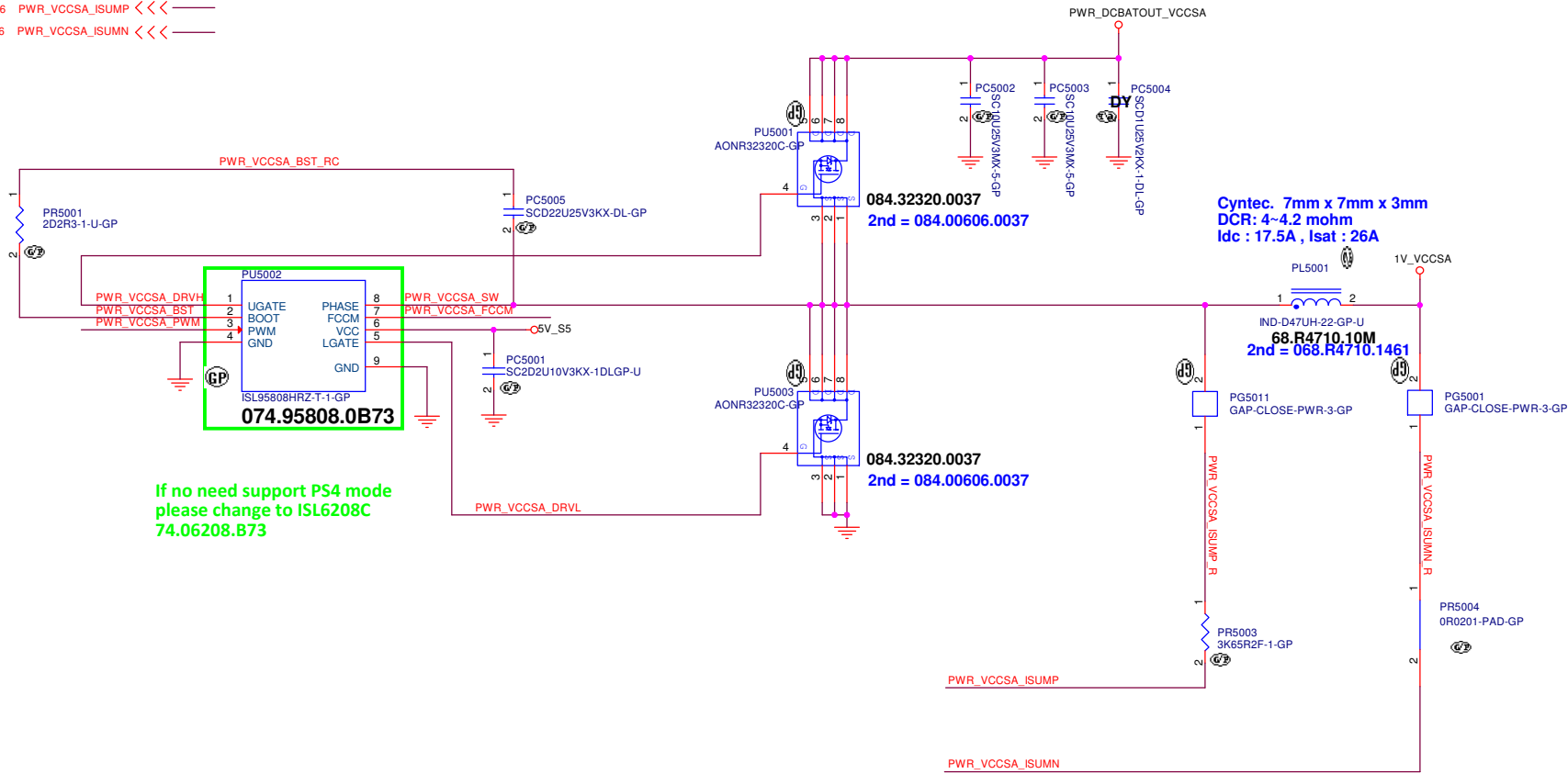
Title		
POWER (CPU VCCGTS RSVD)		
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ISL95808 For VCCSA

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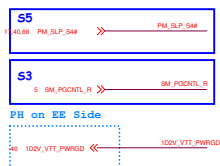
46 PWR_VCCSA_PWM >>>
46 PWR_VCCSA_FCCM >>>
46 PWR_VCCSA_ISUMP <<<
46 PWR_VCCSA_ISUMN <<<



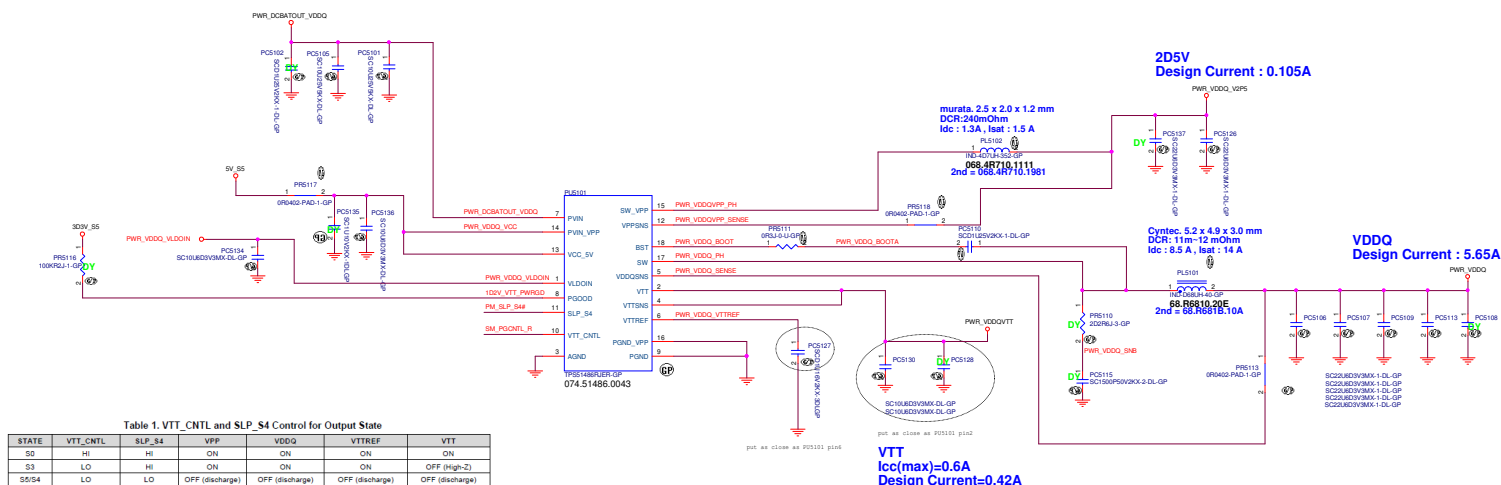
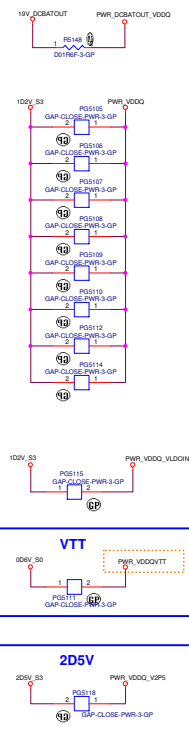
<https://Dr-Bios.com>

SSID = PWR.Plane.Regulator_1D2V/0D6V

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Core Design

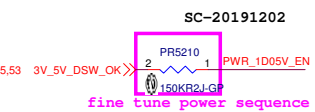
DELL Wistron Corporation
2/F, 88, Sec. 1, Hsu Tai Wu Rd., Tainan, Taiwan, R.O.C.

051 POWER (TPS51486R VDDQ/VTT)

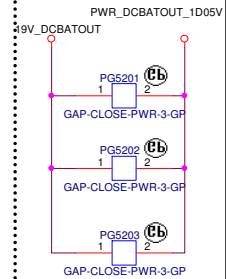
Document Number: MockingBird CML

Rev: SC

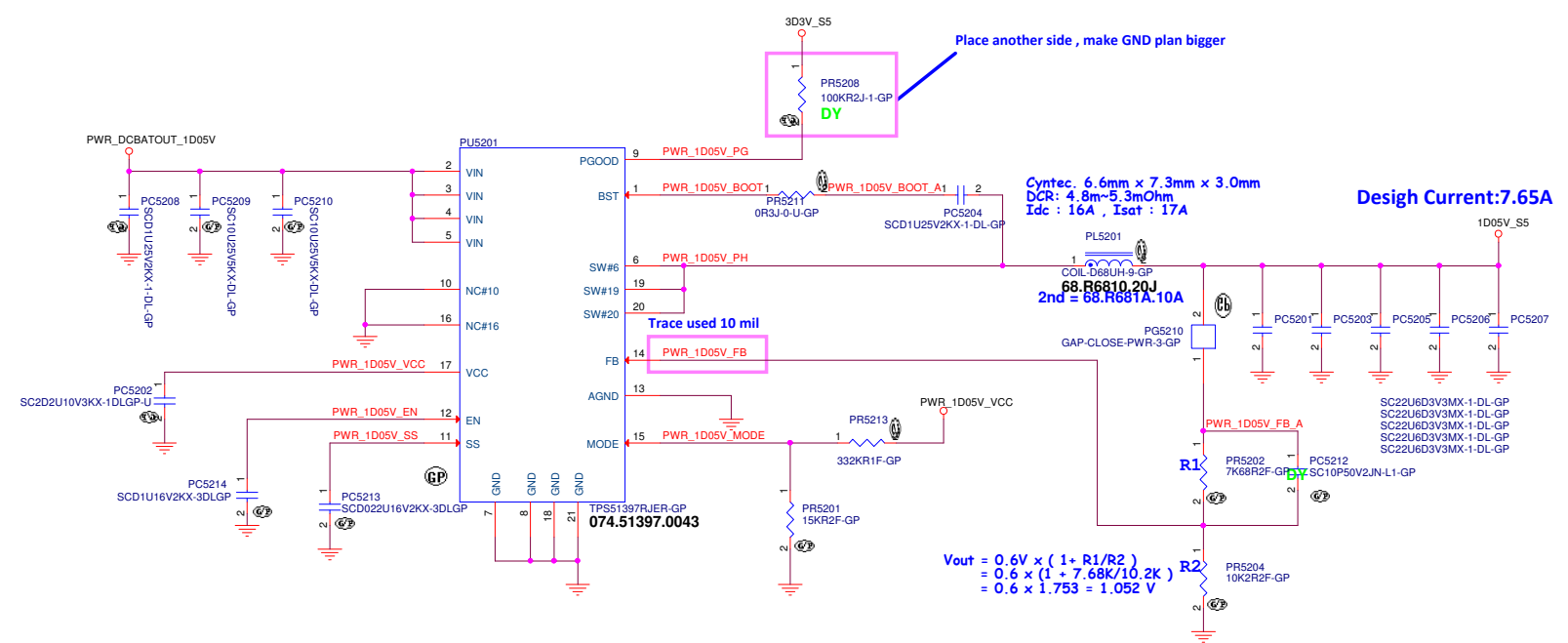
OFFPAGE-Signal



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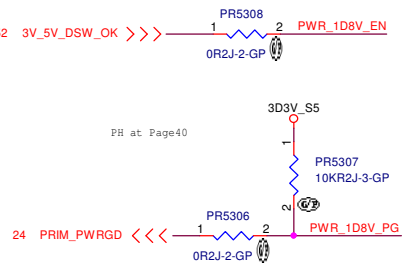


TPS51397 For 1D05V

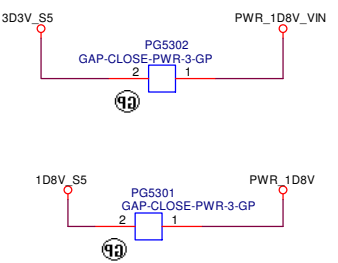


SSID = 1D8V

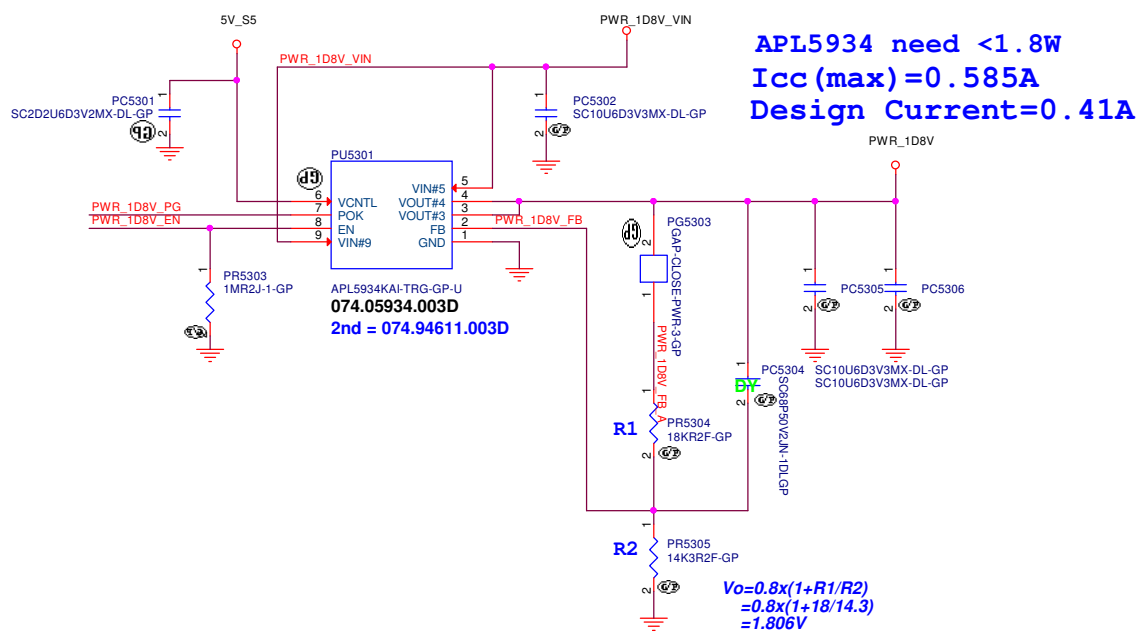
OFFPAGE



OFFPAGE_GAP




APL5934 for 1D8V



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Title

054_LDO-V1D8V&2D5V

Size

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Rev

A3

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Title

CRT(Reserved)

Size

A3

Document Number

Mockingbird_CML

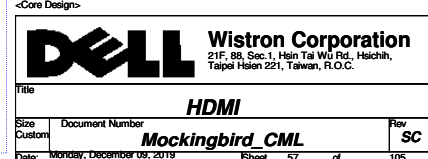
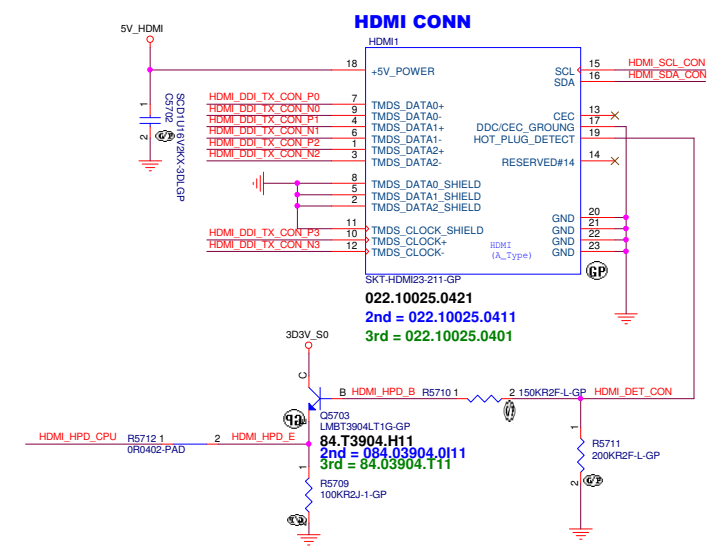
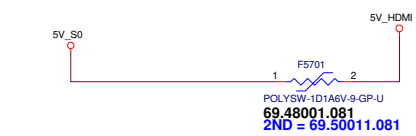
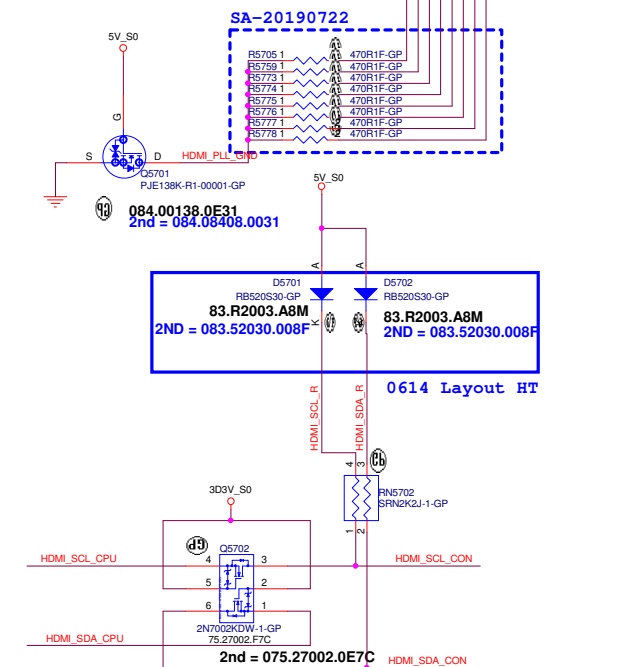
Rev

SC

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Device	Pin	Signal	Function
HDMI DDI TX N3	C5701	1	SCD1U16V2KX-3DLGP
HDMI DDI TX P3	C5704	1	SCD1U16V2KX-3DLGP
HDMI DDI TX N0	C5705	1	SCD1U16V2KX-3DLGP
HDMI DDI TX P0	C5703	1	SCD1U16V2KX-3DLGP
HDMI DDI TX N1	C5707	1	SCD1U16V2KX-3DLGP
HDMI DDI TX P1	C5706	1	SCD1U16V2KX-3DLGP
HDMI DDI TX N2	C5708	1	SCD1U16V2KX-3DLGP
HDMI DDI TX P2	C5709	1	SCD1U16V2KX-3DLGP



(Blanking)

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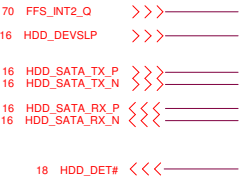
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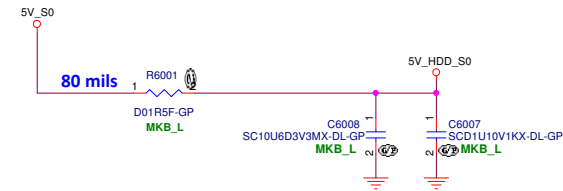
Size	Document Number	Rev
A3	Mockingbird_CML	SC

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HDD

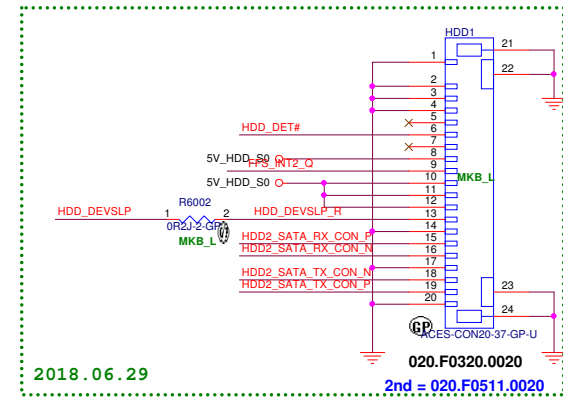
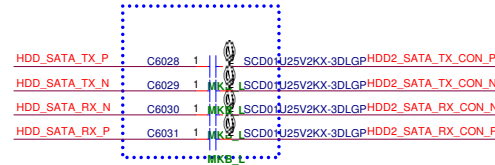


HDD POWER



SATA HDD Connector

COLAY WITH:R1611/R1612/R1607/R1608



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Taipei Hsien 221, Taiwan, R.O.C.

Title **SATA IF_HDD/ODD**

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Custom	Mockingbird CML	SC
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SSID = WLAN

PCIE

16 WLAN_PCIE_TX_N >>>=
16 WLAN_PCIE_TX_P <<<=
16 WLAN_PCIE_RX_N >>>=
16 WLAN_PCIE_RX_P <<<=

PCIE_CLK

18 WLAN_CLK_CPU_N >>>=
18 WLAN_CLK_CPU_P <<<=
18 WLAN_CLKREQ_CPU_N <<<=

USB2.0

16 BT_USB20_P >>>=
16 BT_USB20_N <<<=

Single end

3 BLUETOOTH_EN >>>=

Debug

24,68 HOST_DEBUG_TX >>=

Power EN (Madesimo)

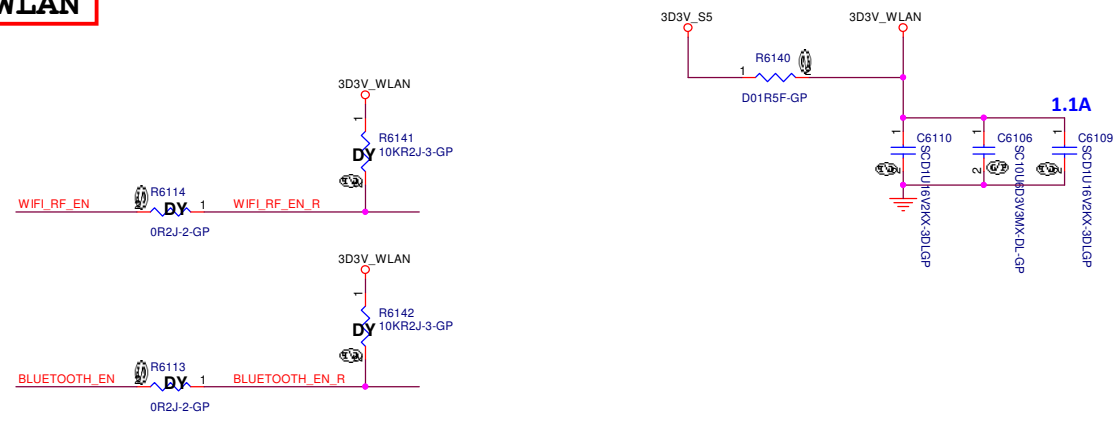
19 BT_PCMOUT_CLKREQ0 >>>=
19 BT_PCMFRM_CRF_RST_N >>>=

21 CNV_WT_DN0 >>>=
21 CNV_WT_DP0 >>>=
21 CNV_WT_DN1 >>>=
21 CNV_WT_DP1 >>>=
21 CNV_WT_CLK_DN >>>=
21 CNV_WT_CLK_DP >>>=

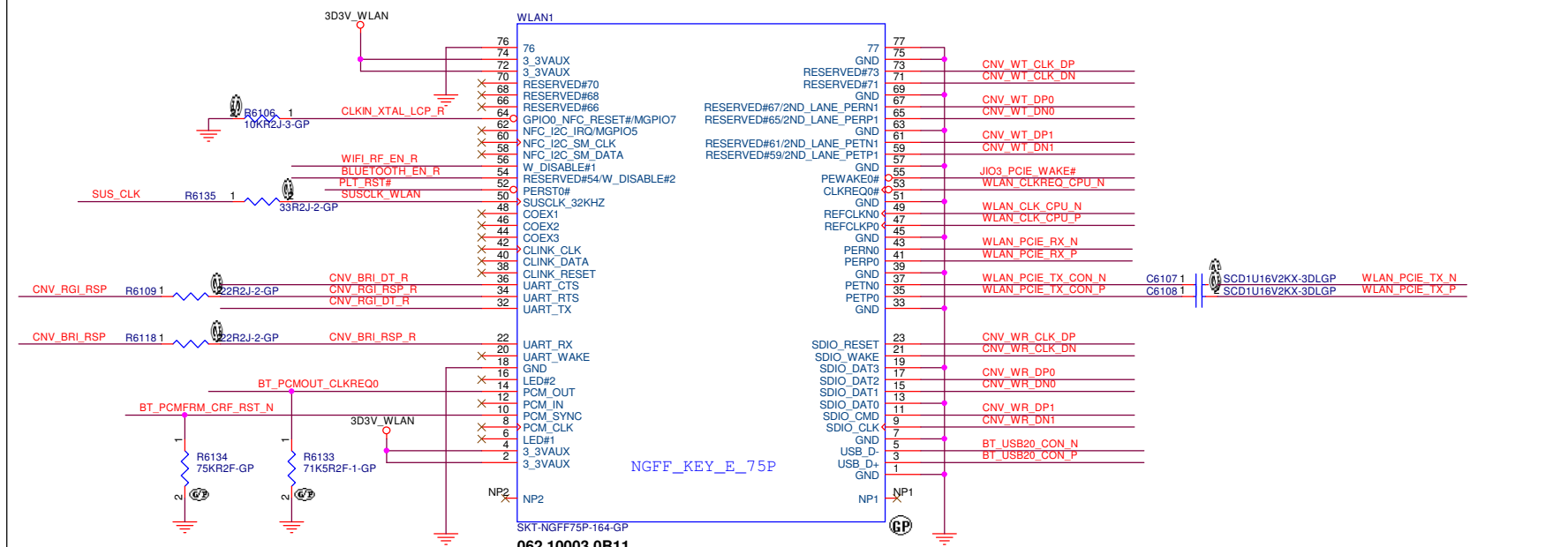
21 CNV_WR_DN0 <<<=
21 CNV_WR_DP0 <<<=
21 CNV_WR_DN1 <<<=
21 CNV_WR_DP1 <<<=
21 CNV_WR_CLK_DN <<<=
21 CNV_WR_CLK_DP <<<=

15,20 CNV_RGI_DT_R >>>=
20 CNV_BRI_DT_R >>>=
20 CNV_BRI_RSP <<<=
20 CNV_RGI_RSP <<<=

18 JIO3_PCIE_WAKE# >>=
18 CLKN_XTAL_LCP_R >>=



AFTE14P-GP	AFTP6101	1	3D3V_WLAN
AFTE14P-GP	AFTP6105	1	WLAN_CLKREQ_CPU_N
AFTE14P-GP	AFTP6106	1	WIFI_RF_EN_R
AFTE14P-GP	AFTP6107	1	BLUETOOTH_EN_R
AFTE14P-GP	AFTP6108	1	PLT_RST#
AFTE14P-GP	AFTP6109	1	BT_USB20_CON_N
AFTE14P-GP	AFTP6110	1	BT_USB20_CON_P
AFTE14P-GP	AFTP6102	1	JIO3_PCIE_WAKE#



SKT-NGFF75P-164-GP
062.10003.0B11
2nd = 062.10007.0371
3rd = 062.10007.0511

BT_USB20_CON_P R6111 2 0R0402-PAD BT_USB20_P
BT_USB20_CON_N R6110 2 0R0402-PAD BT_USB20_N

<Core Design>

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File: **NGFF WLAN CONN**

Size A3 Document Number: **Mockingbird_CML** Rev: **SC**

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```

24 CLK_ITE010    >>>
24 DAT_ITE010    >>>

WWAN

16 WWAN_PCE_RX_N    >>>
16 WWAN_PCE_RX_P    >>>
16 WWAN_PCE_TX_N    >>>
16 WWAN_PCE_TX_P    >>>

18 WWAN_PCE_CLK_P    >>>
18 WWAN_CLKREQ_CPU_N >>>

20 WWAN_FULL_PWR_EN_R >>>

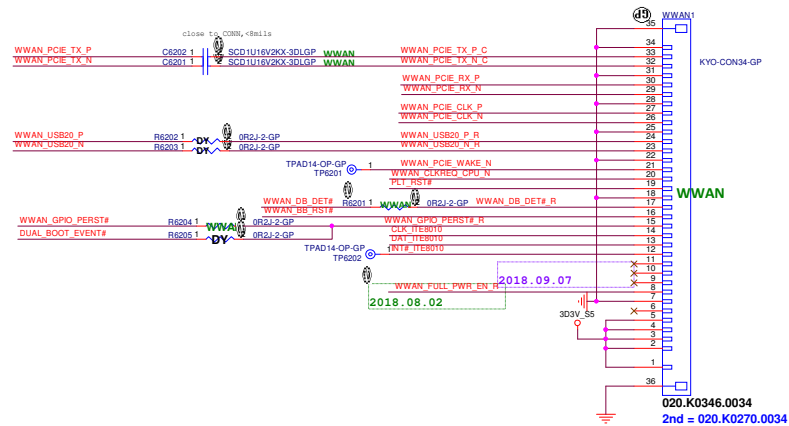
21 WWAN_BB_RST#    >>>
17,40,61,63,66,91 WWAN_GP2_PERST# >>>
                    PLL_RST# >>>

20,21 WWAN_DB_DET#    <<<<

16 WWAN_USB20_N    >>>
16 WWAN_USB20_P    >>>

16 DUAL_BOOT_EVENT# >>>>

```



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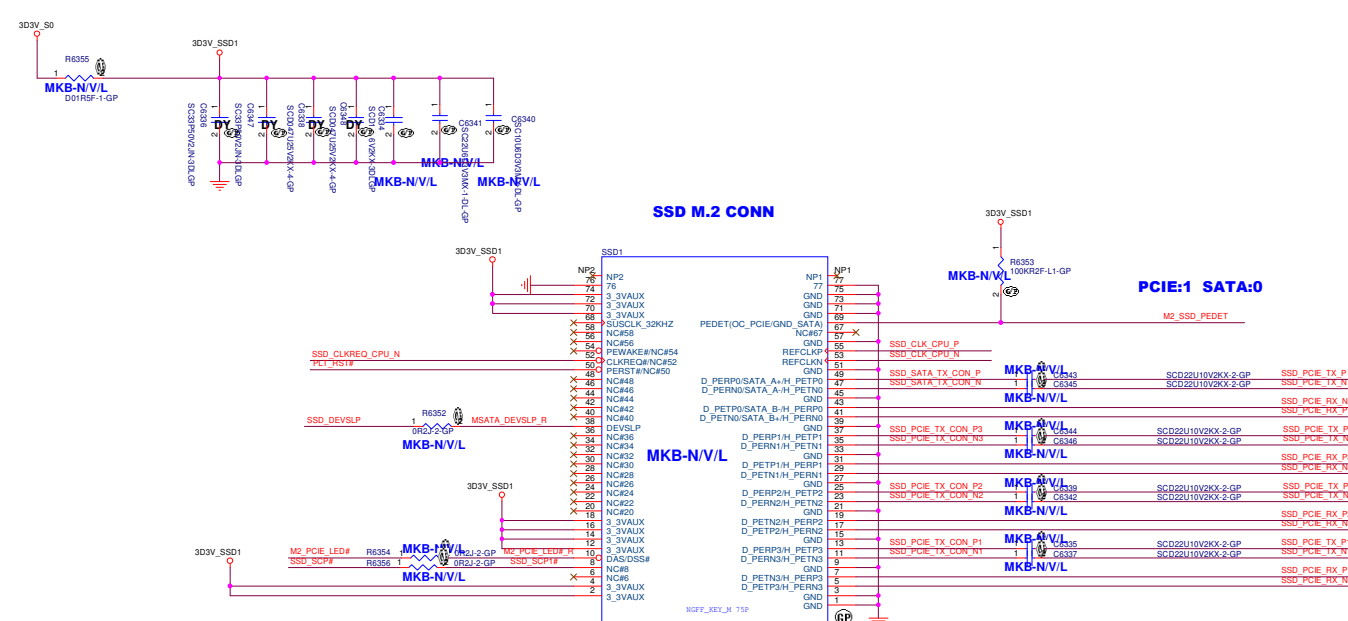
SSID = M.2 SSD

18 SSD_CLKREQ_CPU_N <<<
17,40,61,62,63,66,91 PLT_RST# >>>

16 SSD_DEVSLP >>>
18 SSD_CLK_CPU_P >>>
18 SSD_CLK_CPU_N >>>
16 SSD_PCIE_TX_P >>>
16 SSD_PCIE_TX_N >>>
16 SSD_PCIE_RX_N >>>
16 SSD_PCIE_RX_P >>>
16 SSD_PCIE_TX_P3 >>>
16 SSD_PCIE_RX_N3 >>>
16 SSD_PCIE_TX_P2 >>>
16 SSD_PCIE_TX_N2 >>>
16 SSD_PCIE_RX_P2 >>>
16 SSD_PCIE_RX_N2 >>>
16 SSD_PCIE_TX_P1 >>>
16 SSD_PCIE_TX_N1 >>>
16 SSD_PCIE_RX_P1 >>>
16 SSD_PCIE_RX_N1 >>>

16 M2_SSD_PEDET <<<
64 M2_PCIE_LED# <<<

24 SSD_SCP# >>>



SSD M.2 CONN

PCIE:1 SATA:0

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	SSD1	17	SSD17	33	SSD33	49	SSD49
2	SSD2	18	SSD18	34	SSD34	50	SSD50
3	SSD3	19	SSD19	35	SSD35	51	SSD51
4	SSD4	20	SSD20	36	SSD36	52	SSD52
5	SSD5	21	SSD21	37	SSD37	53	SSD53
6	SSD6	22	SSD22	38	SSD38	54	SSD54
7	SSD7	23	SSD23	39	SSD39	55	SSD55
8	SSD8	24	SSD24	40	SSD40	56	SSD56
9	SSD9	25	SSD25	41	SSD41	57	SSD57
10	SSD10	26	SSD26	42	SSD42	58	SSD58
11	SSD11	27	SSD27	43	SSD43	59	SSD59
12	SSD12	28	SSD28	44	SSD44	60	SSD60
13	SSD13	29	SSD29	45	SSD45	61	SSD61
14	SSD14	30	SSD30	46	SSD46	62	SSD62
15	SSD15	31	SSD31	47	SSD47	63	SSD63
16	SSD16	32	SSD32	48	SSD48	64	SSD64

Table 13-12. SATA / PCI Express® Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2 / SATA	PCI Express® Gen 3 / SATA
Processor Tx	100 nF	220 nF	100 nF	100 nF	220 nF
Processor Rx	None	None	100 nF	None	None

Notes:
1. Design Constraints for PCIe only applications, please refer to the PCIe guidelines for details.
2. Design Constraints for SATA only applications, please refer to the SATA guidelines for details.
3. Design Constraints for SATA / PCIe mixed applications, please refer to the SATA / PCIe guidelines for details.
4. Design Constraints for SATA / PCIe mixed applications, please refer to the SATA / PCIe guidelines for details.
5. Design Constraints for SATA / PCIe mixed applications, please refer to the SATA / PCIe guidelines for details.
6. Design Constraints for SATA / PCIe mixed applications, please refer to the SATA / PCIe guidelines for details.

M.2 SSD2

16 SSD_PCIE_TX_P9 >>>
16 SSD_PCIE_TX_N9 >>>
16 SSD_PCIE_RX_N9 >>>
16 SSD_PCIE_RX_P9 >>>

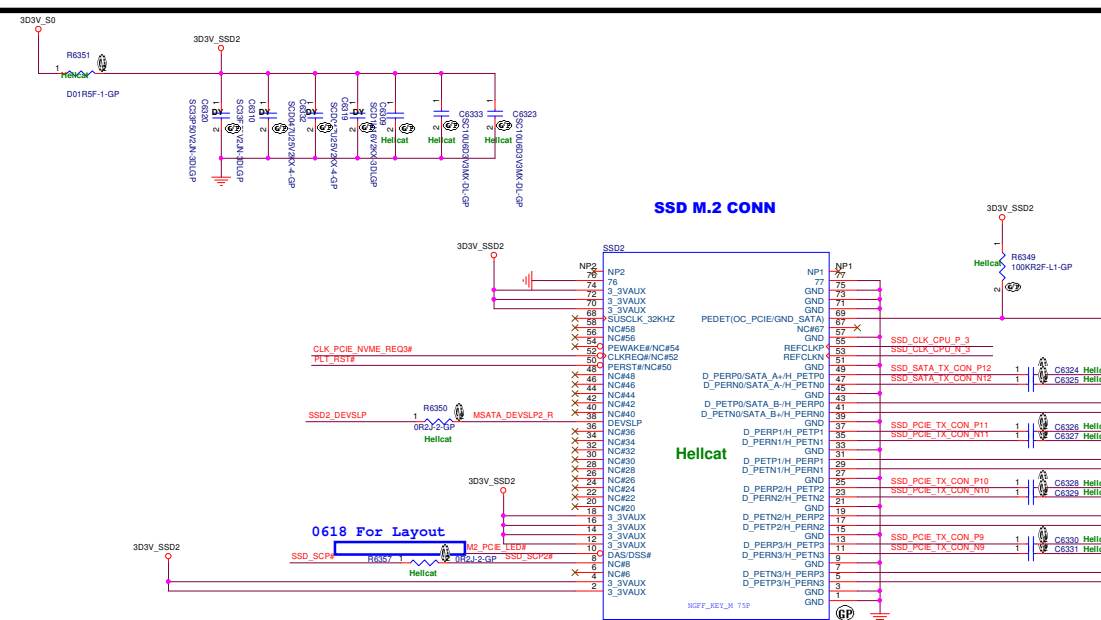
16 SSD_PCIE_TX_P10 >>>
16 SSD_PCIE_TX_N10 >>>
16 SSD_PCIE_RX_N10 >>>
16 SSD_PCIE_RX_P10 >>>

16 SSD_PCIE_TX_P11 >>>
16 SSD_PCIE_TX_N11 >>>
16 SSD_PCIE_RX_N11 >>>
16 SSD_PCIE_RX_P11 >>>

16 SSD_PCIE_TX_P12 >>>
16 SSD_PCIE_TX_N12 >>>
16 SSD_PCIE_RX_N12 >>>
16 SSD_PCIE_RX_P12 >>>

16 SSD_CLK_CPU_P_3 >>>
16 SSD_CLK_CPU_N_3 >>>
16 CLK_PCIE_NVME_REQ3M >>>
17,40,61,62,63,66,91 PLT_RST# >>>

16 SSD2_DEVS LP >>>
16 M2_SSD2_PEDET >>>



SSD M.2 CONN

PCIE:1 SATA:0

«Core Design»

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File: **mSATA**

Size: A2 Document Number: **Mockingbird_CML** Rev: **SC**

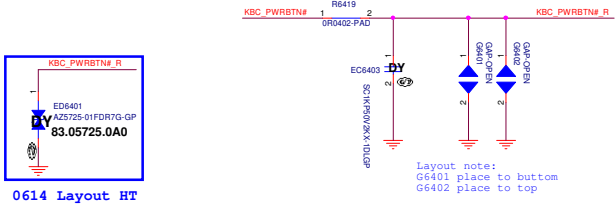
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SSID = Power BTN

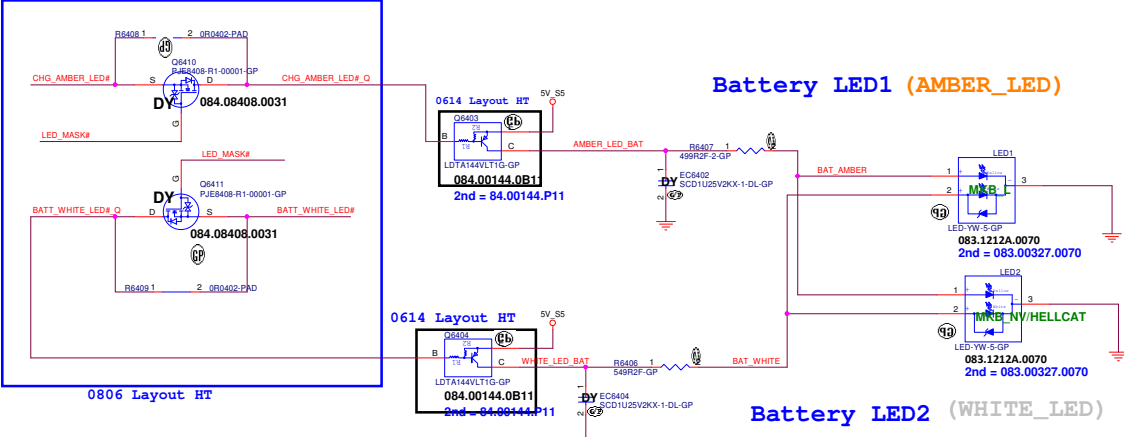
Power button

24 KBC_PWRBTN# <<< _____
66 KBC_PWRBTN#_R <<< _____



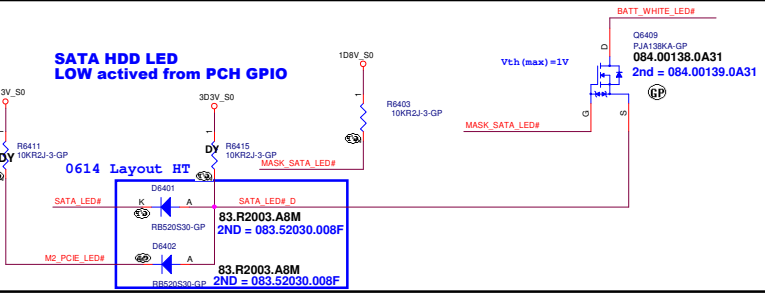
SSID = Battery LED

Low active from KBC GPIO
24,66 LED_MASK# >>> _____
24 CHG_AMBER_LED# >>> _____
24 BATT_WHITE_LED# >>> _____



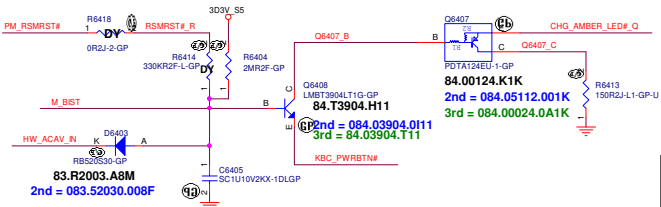
SSID = HDD LED

24 MASK_SATA_LED# >>> _____
16 SATA_LED# >>> _____
63 M2_PCE_LED# <<< _____



SSID = M-BIST

17 PM_RSMRST# >>> _____
24 M_BIST >>> _____
24,44 HW_ACAV_IN >>> _____



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SSID = IO Connector

IO DET

20 IO_DB_DET#_GPP05 <<<

AUDIO

27,29 AUD_RING <<<
27,29 AUD_SLEEVE <<<
29 AUD_HP1_JACK_L1 <<<
29 AUD_HP1_JACK_R1 <<<
27 AUD_SENSE >>>

CRD

16 CARD1_USB20_N <<<
16 CARD1_USB20_P <<<
20 SD_READ_MODE# >>>

USB3.0

PORT1

16 USB2_USB30_RX_N <<<
16 USB2_USB30_RX_P <<<
16 USB2_USB30_TX_N <<<
16 USB2_USB30_TX_P <<<
16 USB2_USB20_N <<<
16 USB2_USB20_P <<<

USB CONTROL

16 USB_OC# <<<
24,35 USB_PWR_EN# <<<

LAN

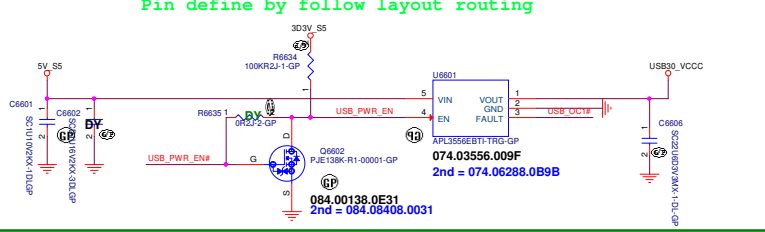
16 LAN_PCIE_RX_N <<<
16 LAN_PCIE_RX_P <<<
16 LAN_PCIE_TX_N <<<
16 LAN_PCIE_TX_P <<<
18 LAN_CLK_CPU_N <<<
18 LAN_CLK_CPU_P <<<
18 LAN_CLKREQ_CPU_N <<<
24 PM_LAN_ENABLE >>>
24 PCIE_LAN_WAKE# >>>
16 LOM_CABLE_DETECT# <<<

FP

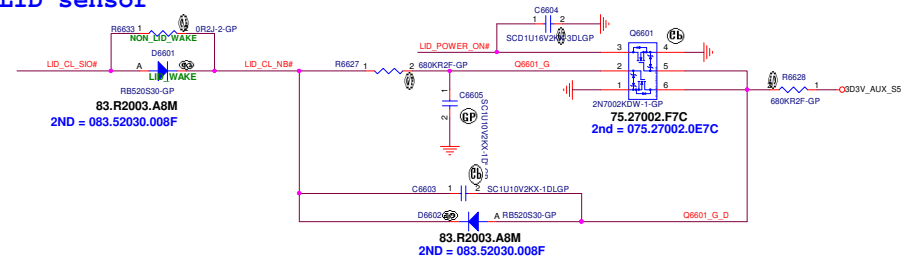
16 FP1_USB20_N <<<
16 FP1_USB20_P <<<
24 FPR_SCAN# >>>
64 KBC_PWRBTN#_R <<<
17,40,51 PM_SLP_S# >>>

20,24 LID_CL_SIO# <<<
24 LID_POWER_ON# >>>
20,24 LID_CL_SIO_TAB# <<<
17,40,61,62,63,91 PLT_RST# <<<
24,64 LED_MASK# >>>
20,65 CPU_IC_SCL_P0 <<<
20,65 CPU_IC_SDA_P0 <<<
44 PWR_CHG_CSOP_R <<<
44 PWR_CHG_CSOP_N <<<
55 3D3V_LCDVDD_R >>>

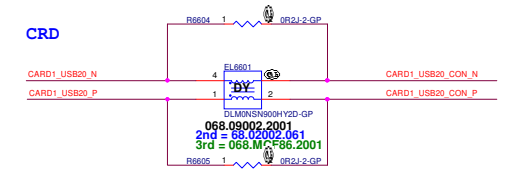
USB2.0 Power



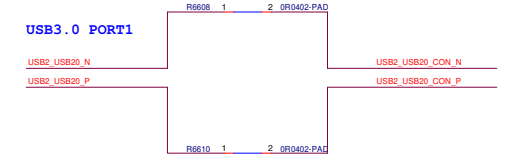
LID sensor



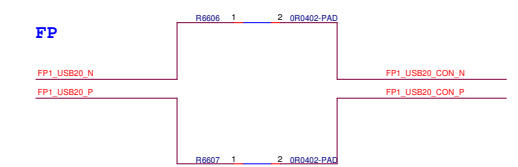
CRD



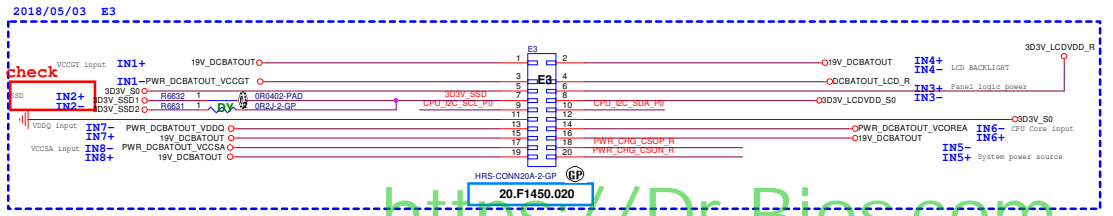
USB3.0 PORT1



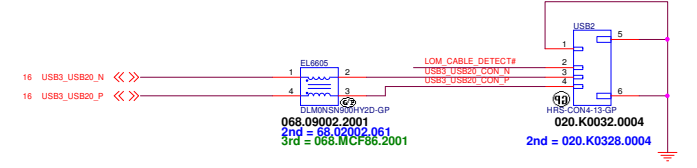
FP



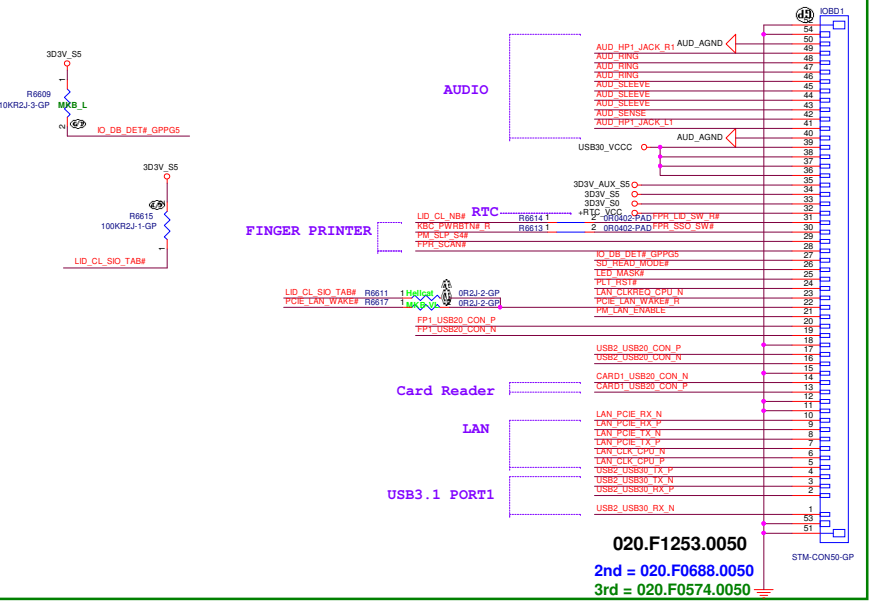
0514 double check



USB2.0 PORT



I/O Board Connector



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IO Board Connector

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ESPI

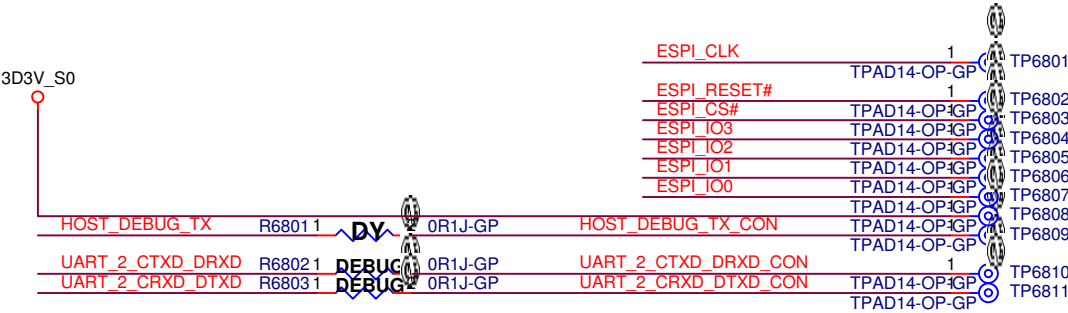
18,24 ESPI_CLK >>> _____
18,24 ESPI_RESET# >>> _____
18,24 ESPI_CS# >>> _____

18,24 ESPI_IO[3..0] <<>> _____
ESPI_IO3 _____
ESPI_IO2 _____
ESPI_IO1 _____
ESPI_IO0 _____


UART

24 HOST_DEBUG_TX >>> _____
20 UART_2_CTXD_DRXD >>> _____
20 UART_2_CRXD_DTXD <<< _____

ESPI Debug Connector



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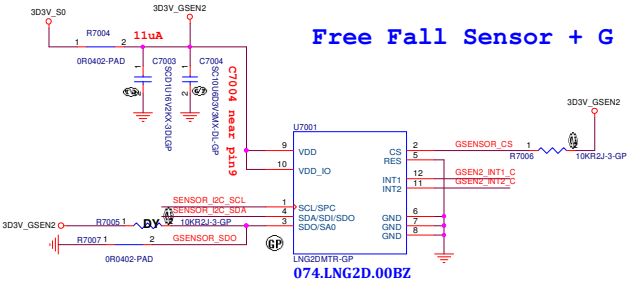
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Title			
Reserved			
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SSID = Free Fall sensor

Mantis Accelerometer for adaptive thermal and HDD protection

The slave address (SAD) associated to the **LNG2DM** is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device **address**. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

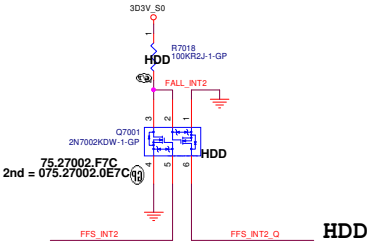
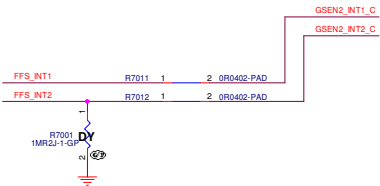
Free Fall Sensor + G Sensor



Hellcat & MKB-L (8bit) : 074.LNG2D.00BZ
MKB-N/V (12bit) : 074.LIS2D.M002

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:


- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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SSID =TypeC

74 PD_VBUS_C_CTRL1 <<< _____

EC

24 TYPEC_SMBDA >>> _____

24 TYPEC_SMBCLK >>> _____

74 VBUS_P_CTRL <<< _____

24 CCG5C_IC_INT# >>> _____

0513

MUX TUSB546

73 IC_DATA_PD >>> _____

73 IC_CLK_PD >>> _____

4.73 DP1_HPD_CPU <<< _____

73 CCG5_SBU1 <<< _____

73 CCG5_SBU2 <<< _____

74 NXSP393_FO >>> _____

TYPE-C CONNECTOR

73 USB1_CC1 >>> _____

73 USB1_CC2 >>> _____

73 TOP_MUX_P_L <<< _____

73 TOP_MUX_N_L <<< _____

73 BOT_MUX_P_L <<< _____

73 BOT_MUX_N_L <<< _____

73 USB1_SBU1 <<< _____

73 USB1_SBU2 <<< _____

PCH

16 USB4_USB20_P >>> _____

16 USB4_USB20_N >>> _____

From System

303V_S5 A Q7202 K VCC3PD_1

SBA0520Q-R1-00001-GP-U

083.00520.0F8F

2nd = 083.05S40.001F

303V_S5 A Q7203 K VCC3PD VDDO

SBA0520Q-R1-00001-GP-U

083.00520.0F8F

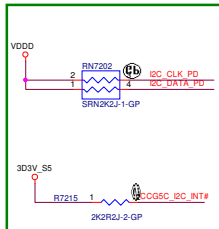
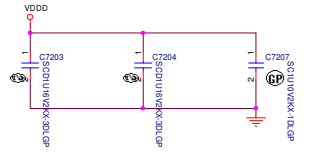
2nd = 083.05S40.001F

For debattery

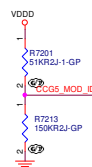
R7210 2 VDDO

0R0402-PAD

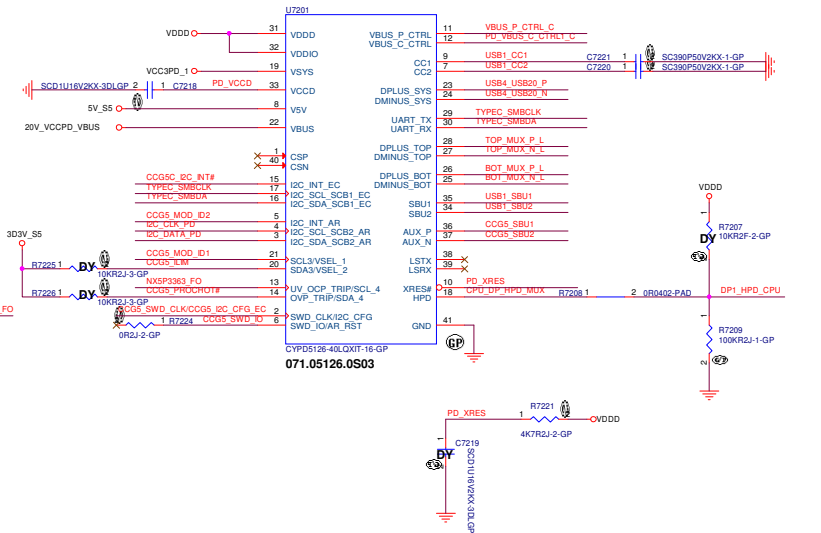
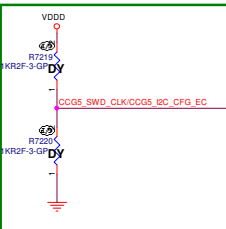
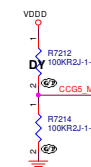
Power



MOD ID Settings



MOD ID Settings



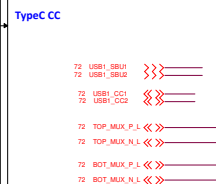
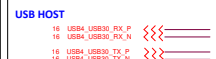
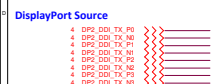
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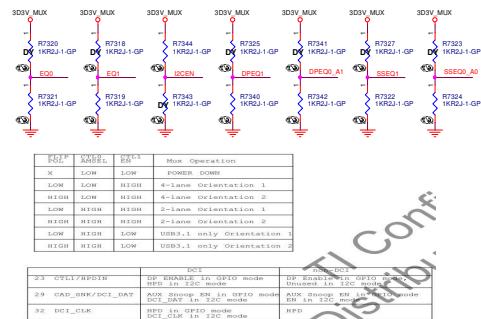
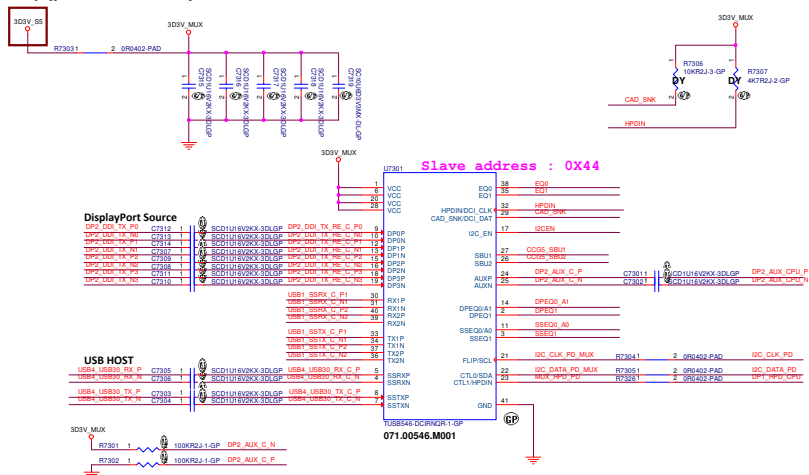
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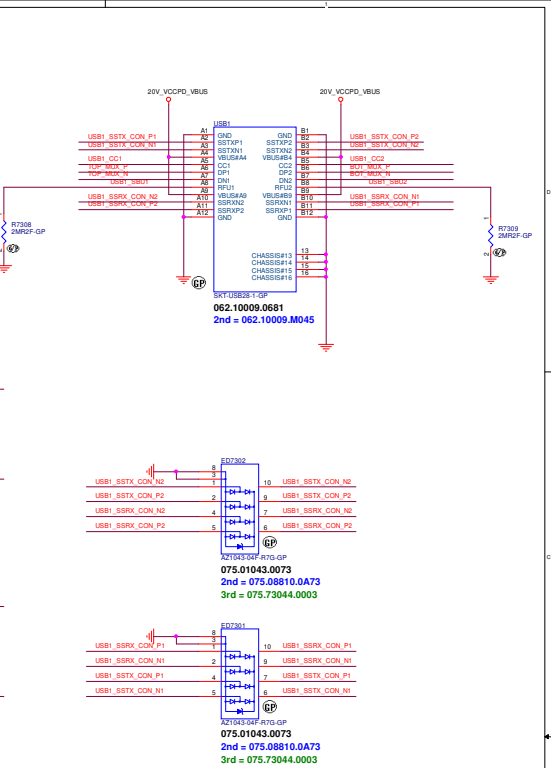
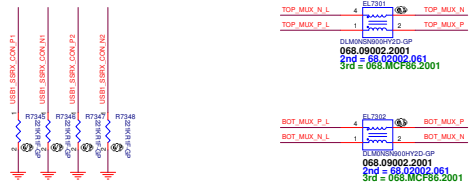
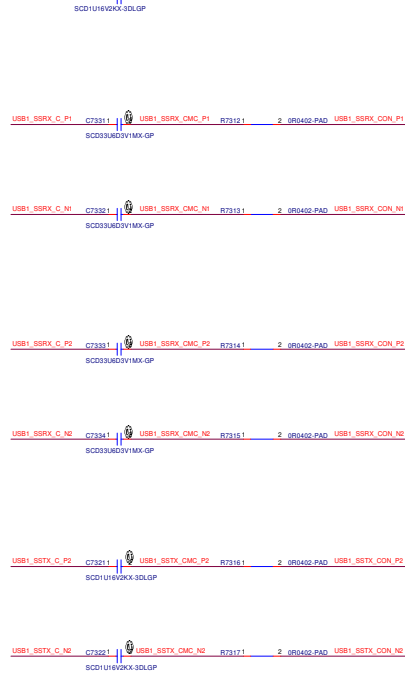
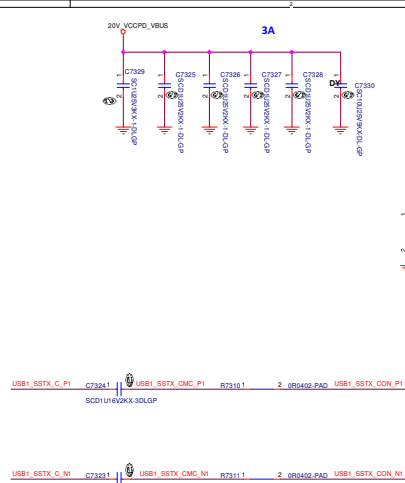
SSID = TYPEC MUX



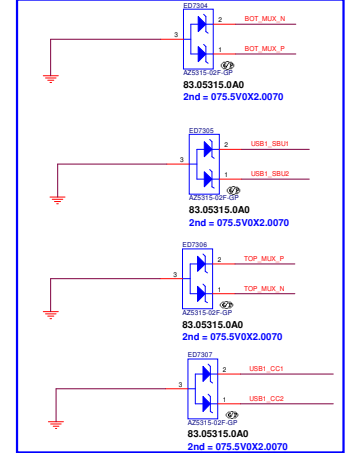
For displayport function at dead battery condition

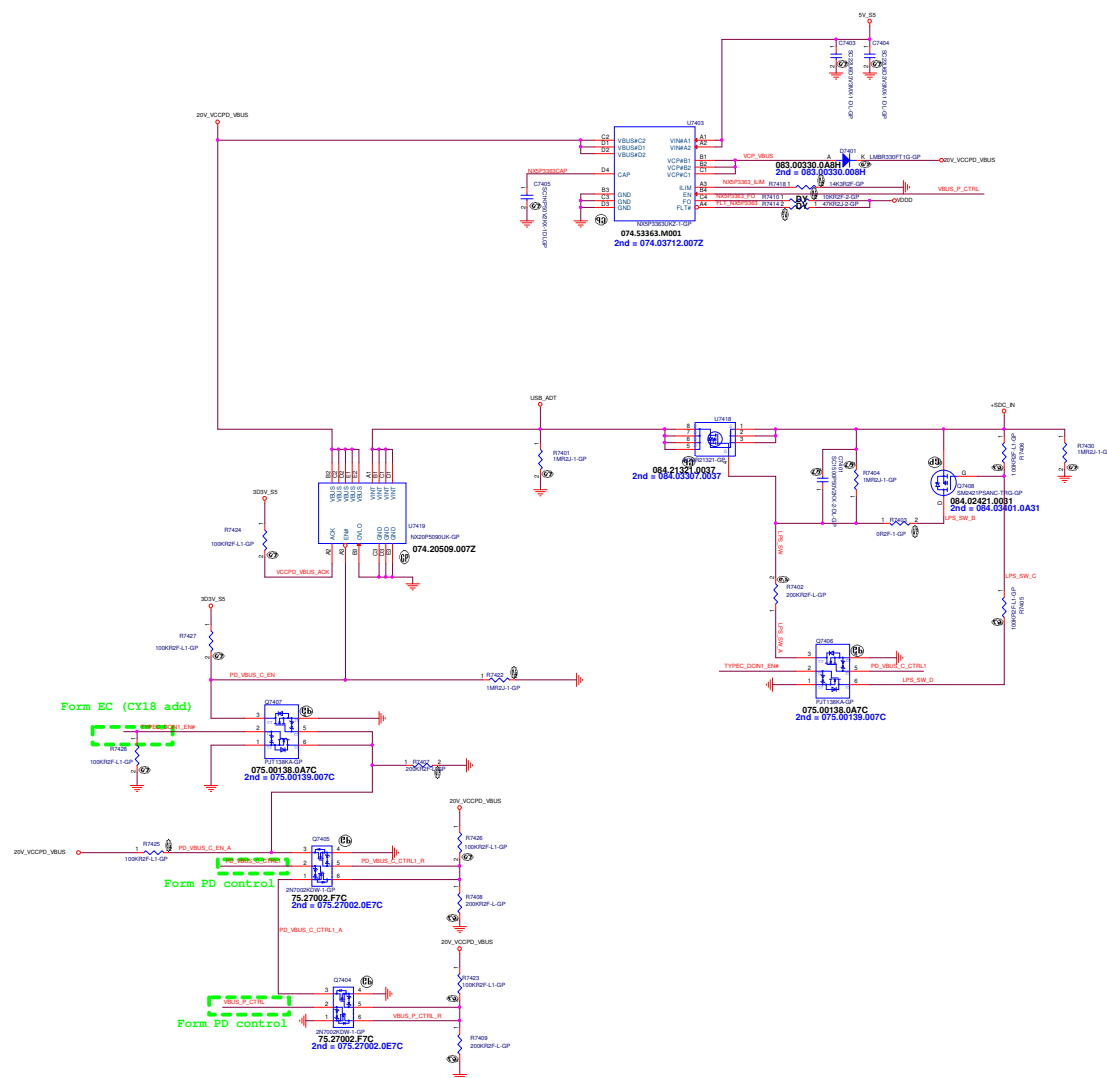


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0614 Layout HT





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File GPU(1/5)PEG	
Size	Document Number
Content	Mockingbird CML
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Title			
GPU(2/5)DIGITALOUT			
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B				B
A				A
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GPU(5/5)PWR/GND

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File		GPU-VRAM1.2 (1/4)	
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File		GPU-VRAM3.4 (2/4)	
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GPU-VRAM5,6 (3/4)

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GPU-VRAM7,8 (4/4)

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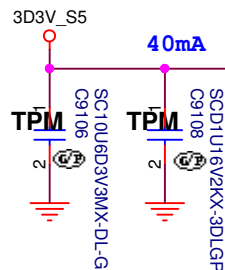
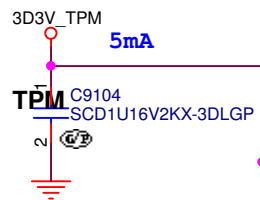
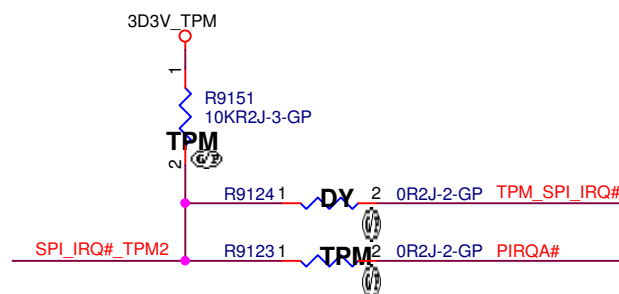
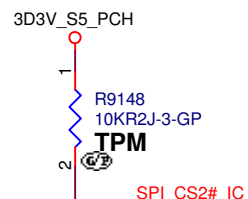
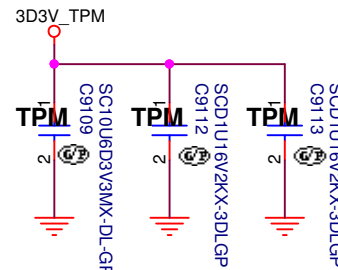
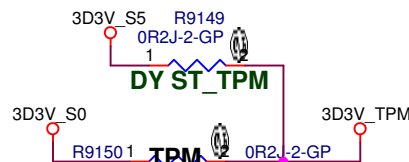
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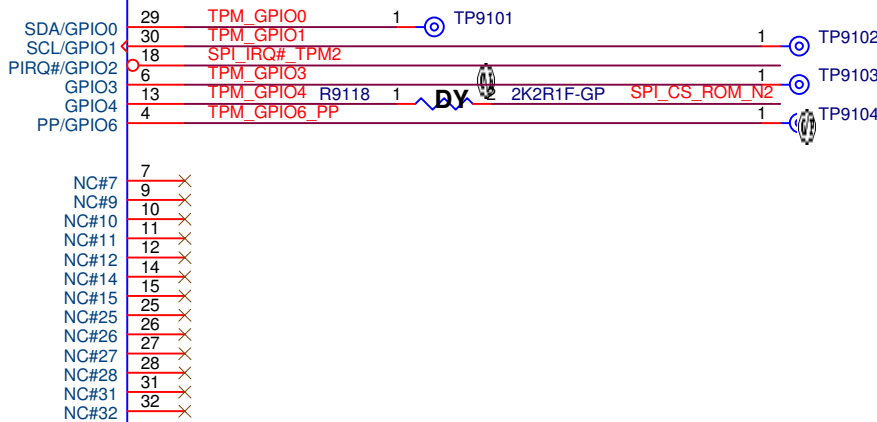
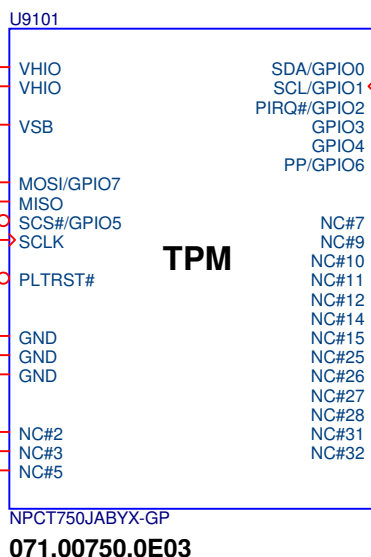
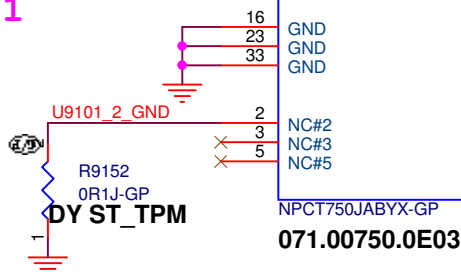
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Title			
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SSID = TPM

17,40,61,62,63,66 PLT_RST# >>>—
 18,24,25 SPI_CLK_ROM >>>—
 15,18,24,25 SPI_SI_ROM >>>—
 18,24,25 SPI_SO_ROM >>>—
 18 SPI_CS_ROM_N2 >>>—
 20 PIRQA# >>>—
 18 TPM_SPI_IRQ# >>>—



Close to U2501



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Title **INT IO (TPM)**

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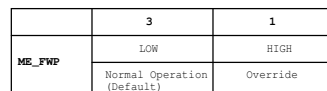
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Size A4	Document Number Mockingbird CML		Rev SC
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19 ME_FWP_SW>>>_____
24 ME_FWP    <<<_____

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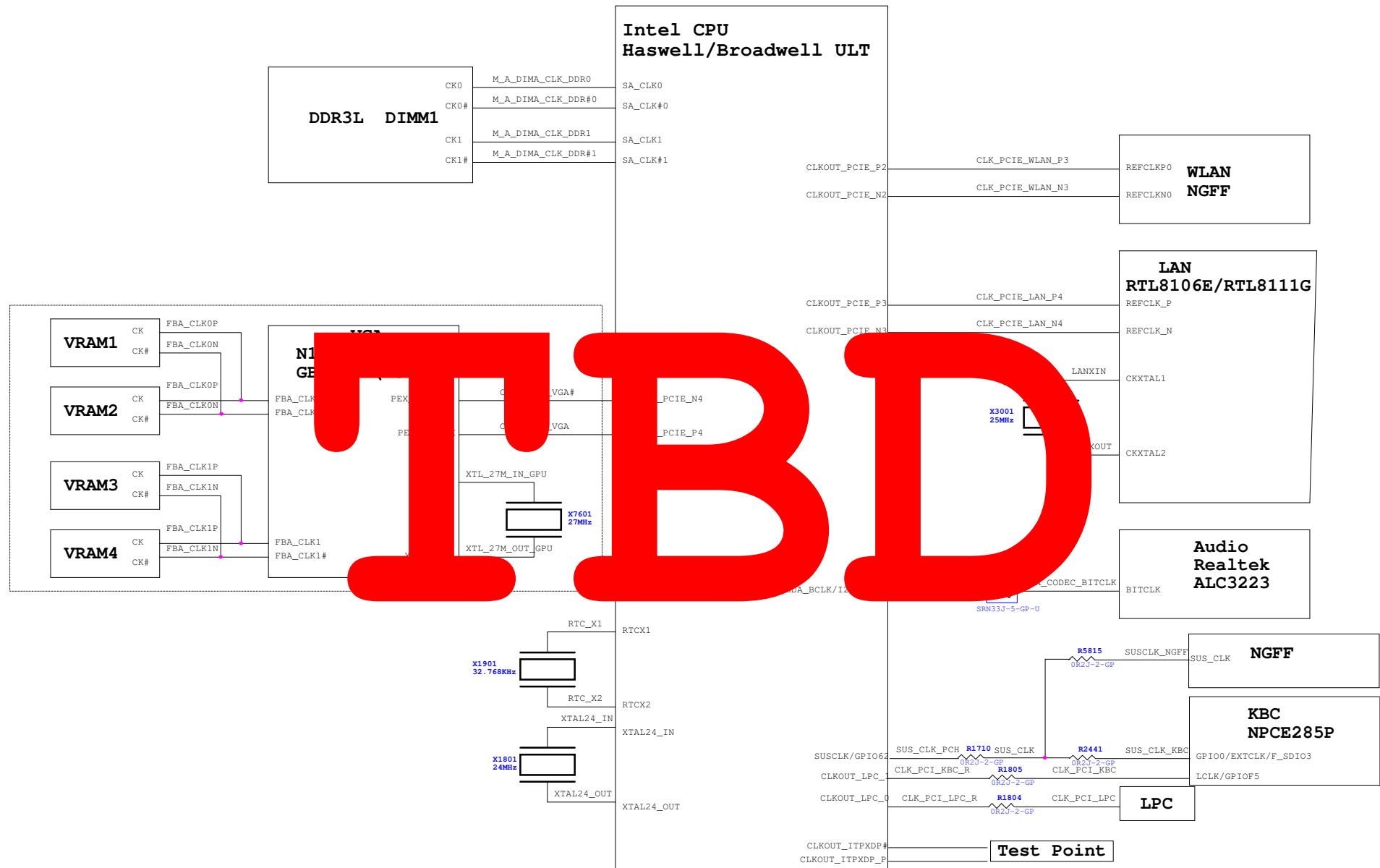


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CLK Block Diagram



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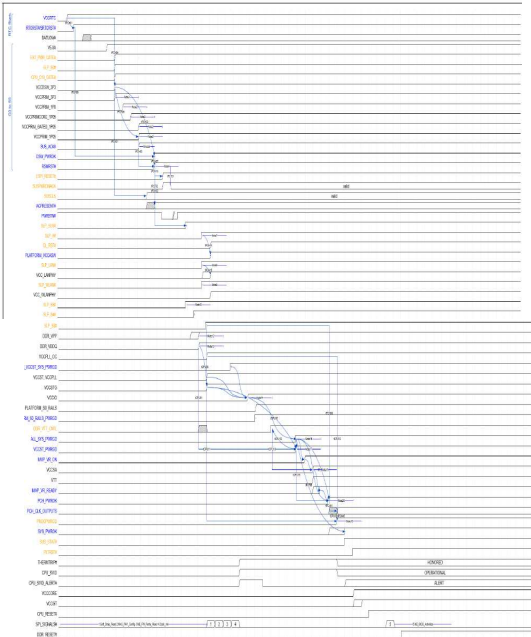
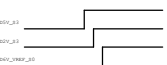
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Date: <i>Monday, December 09, 2019</i>		Sheet 101 of 105	

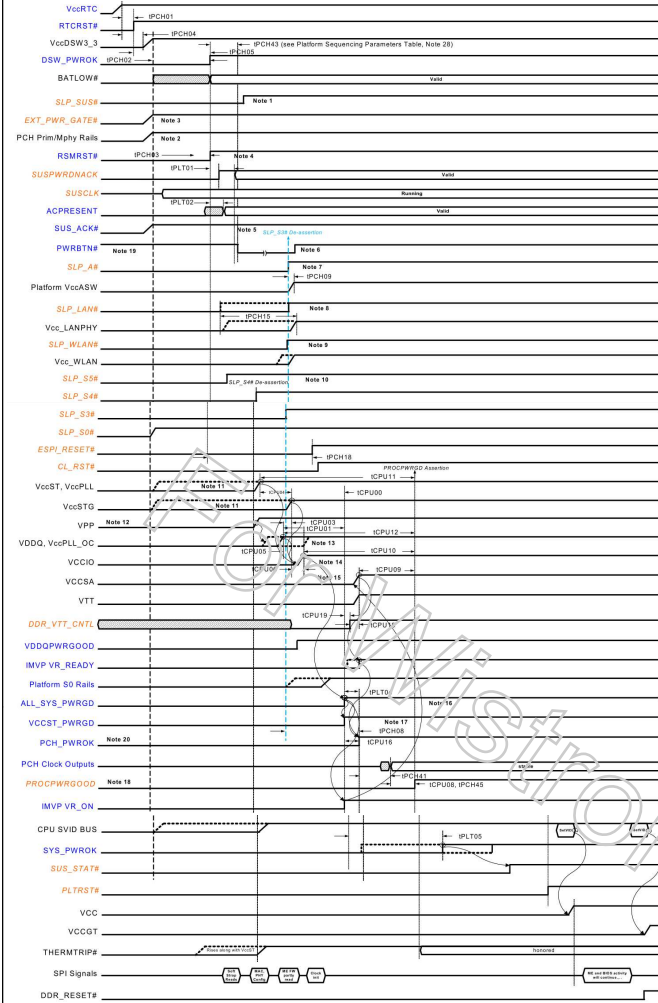
Figure 12-19.WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



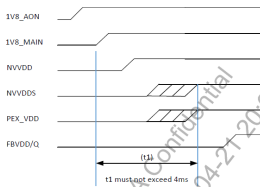
For DDR4 power sequence



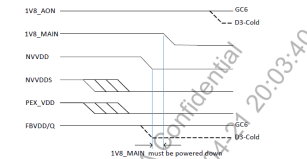
KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



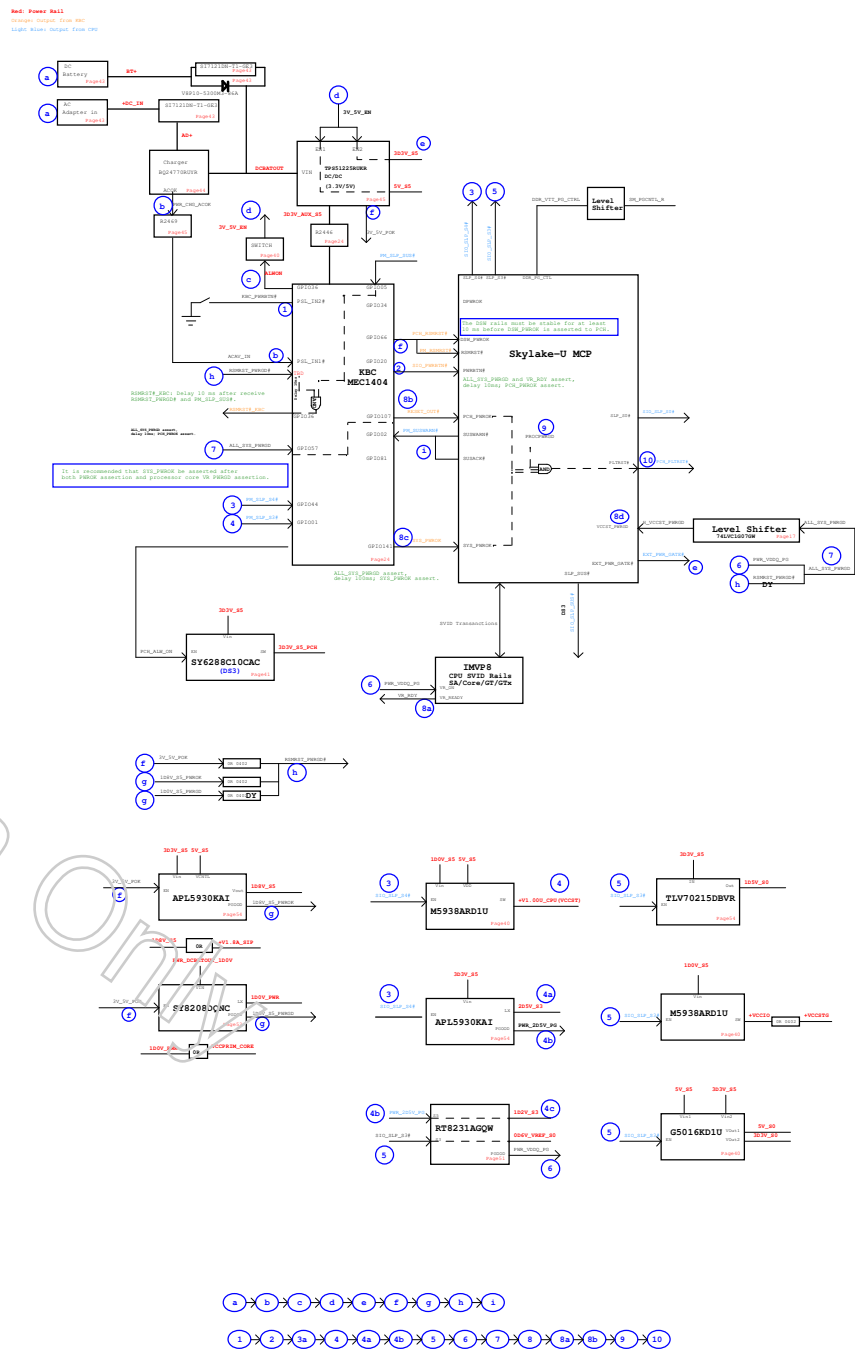
NV N17S GPU Power ON sequence

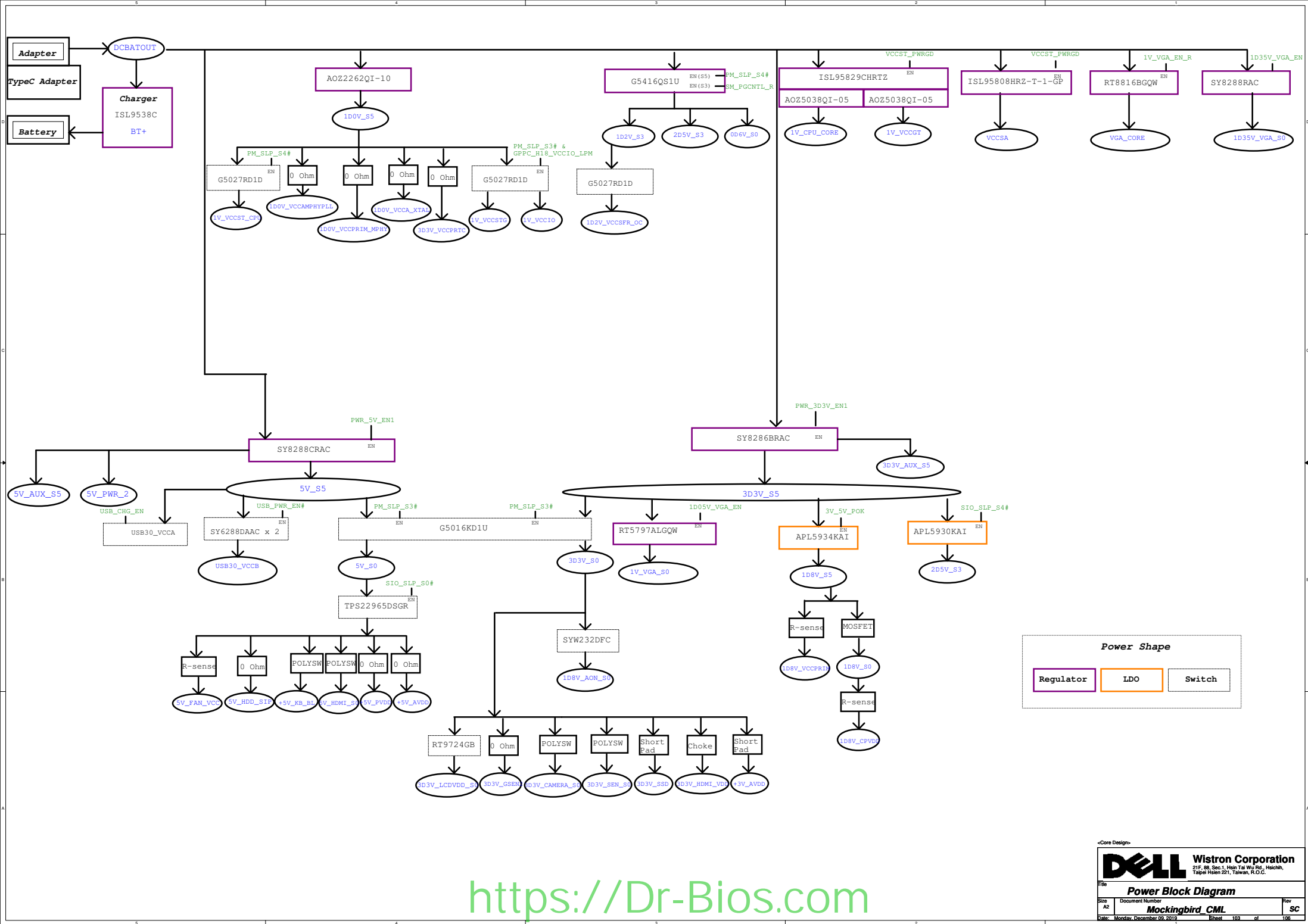


NV N17S GPU Power Down sequence



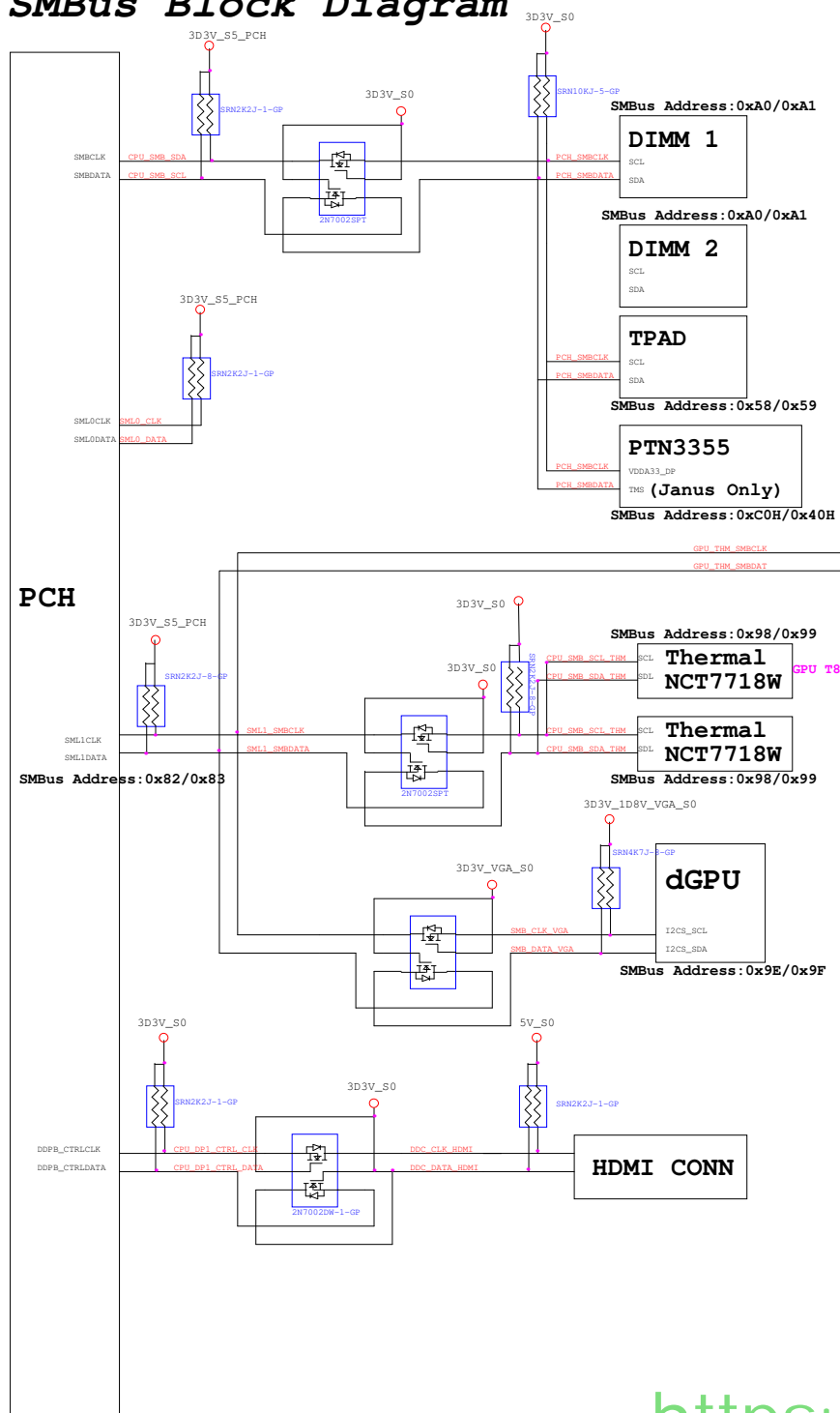
Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



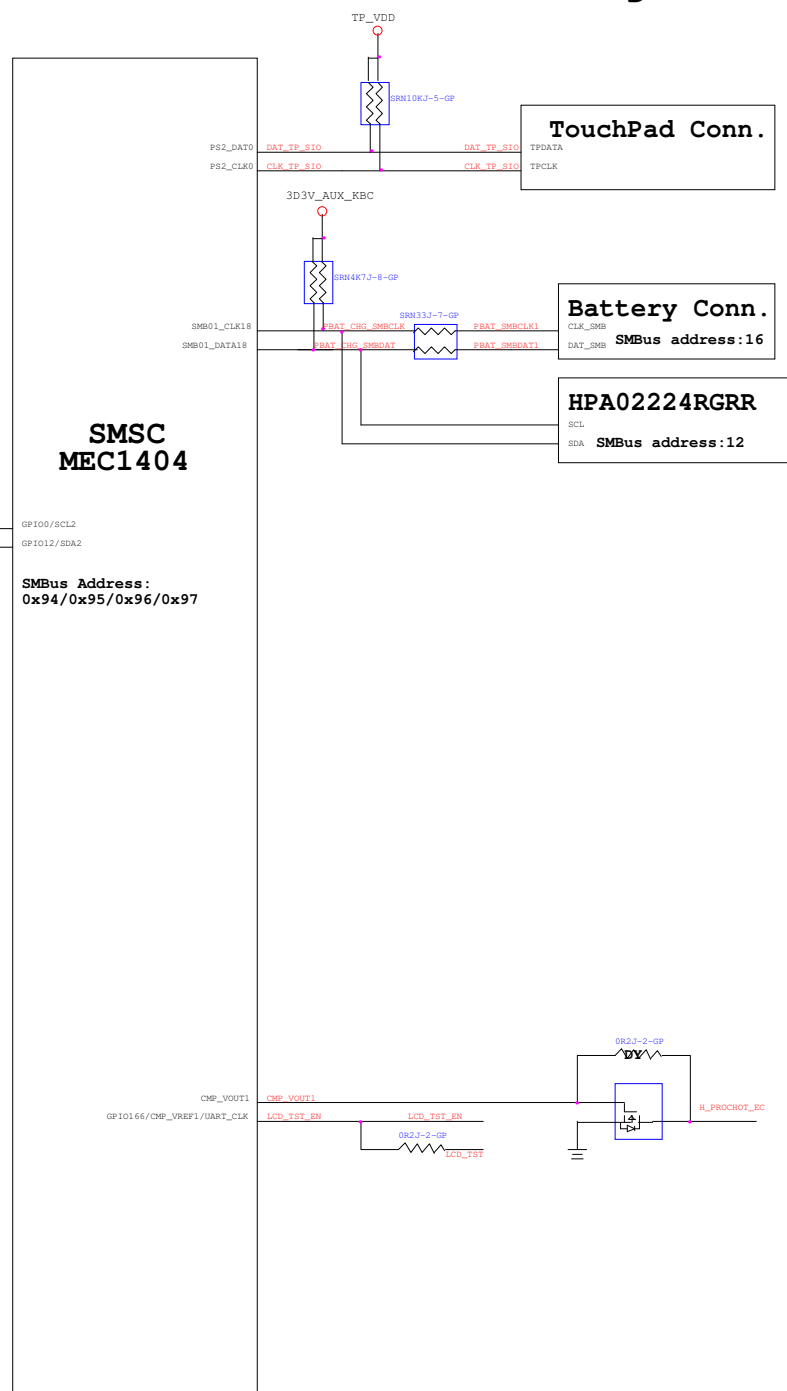


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PCH SMBus Block Diagram

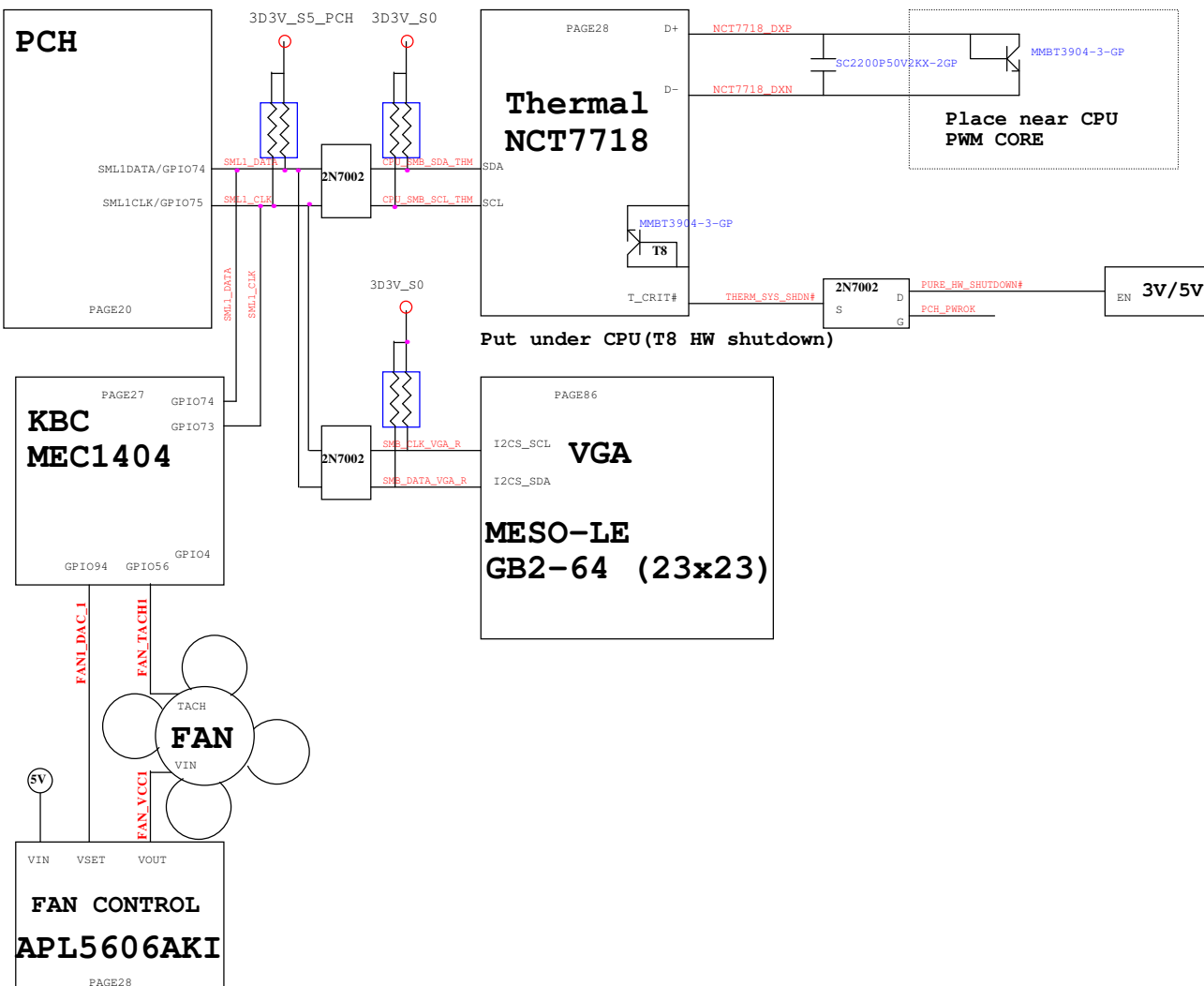


KBC SMBus Block Diagram

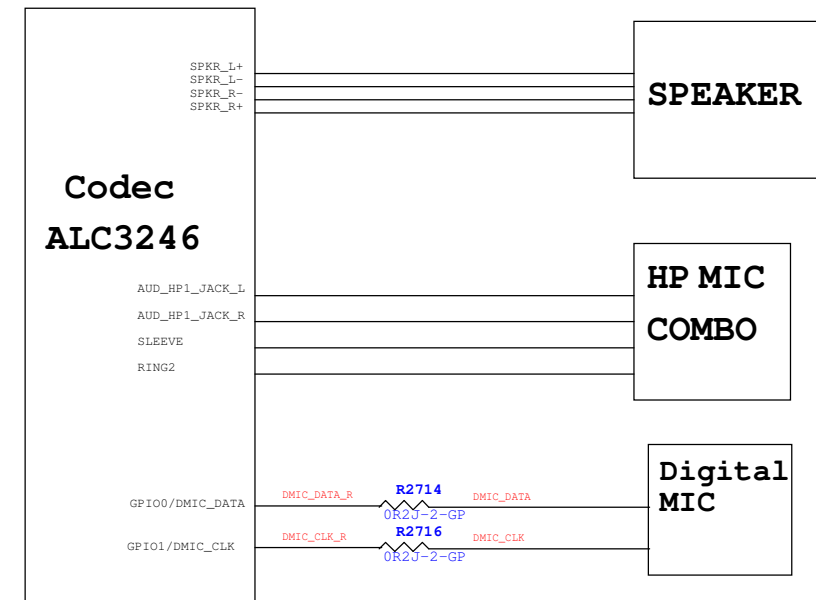


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Thermal Block Diagram



Audio Block Diagram



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